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References

- [1] Jais Abraham et al. Test Methodology Framework for Embedded Core Based Systems. In *Digest of Papers of IEEE International Workshop on Testing Embedded Core-Based Systems (TECS)*, pages 3.4–1–5, Montreal, Canada, May 2000.
- [2] Saman Adham et al. Preliminary Outline of IEEE P1500 Scalable Architecture for Testing Embedded Cores. In *Proceedings IEEE VLSI Test Symposium (VTS)*, pages 483–488, Dana Point, CA, USA, April 1999.
- [3] Advanced RISC Machines Ltd. *The ARM7TDMI Debug Architecture*, December 1995. ARM DAI 0028A, <http://www.arm.com/Documentation/AppNotes/Apps28vA>.
- [4] Joep Aerts. Test Time Reduction Algorithms for Core-Based ICs. Master's thesis, Eindhoven University of Technology, Eindhoven, The Netherlands, April 1998.
- [5] Joep Aerts and Erik Jan Marinissen. Scan Chain Design for Test Time Reduction in Core-Based ICs. In *Proceedings IEEE International Test Conference (ITC)*, pages 448–457, Washington, DC, USA, October 1998.
- [6] Rob Aitken and Fidel Muradali. Trends in SLI Design and their Effect on Test. In *Proceedings IEEE International Test Conference (ITC)*, pages 628–637, Atlantic City, NJ, USA, September 1999.
- [7] Alexandre M. Amory, Leandro A. Oliveira, and Fernando G. Moraes. Software-Based Test for Non-Programmable Cores in Bus-Based System-on-Chip Architectures. In *Proceedings IFIP International Conference on Very Large Scale Integration (VLSI-SOC)*, pages 174–179, Darmstadt, Germany, December 2003.
- [8] Thomas Anderson. This is Hard Core. *Test - The European Test Industry Journal*, Vol. 25(No. 5):S–5–6, June 1999.

- [9] David Appelo et al. Full Built-In Self-Test Solution for System-on-Chip. In *Digest of Papers of IEEE International Workshop on Testing Embedded Core-Based Systems (TECS)*, pages 1.2–1–5, Marina del Rey, CA, USA, May 2001.
- [10] Robert Arendsen and Maurice Lousberg. Core Based Test for a System on Chip Architecture Framework. In *Digest of Papers of IEEE International Workshop on Testing Embedded Core-Based Systems (TECS)*, pages 5.1–1–8, Washington, DC, USA, October 1998.
- [11] William D. Atwell, William C. Bruce Jr., and Grady L. Giles. Tester On A Chip (TOAC) or Apparatus for Application of Tests for Embedded Test Points. *Motorola Technical Developments*, Vol. 9:21–25, August 1989.
- [12] Marcel Baláž and Elena Gramatová. Optimization Techniques for Parallel Interface of Test Wrapper for Embedded Cores. In *Digest of Papers of IEEE European Test Workshop (ETW)*, pages 25–26, Maastricht, The Netherlands, May 2003.
- [13] Luis Basto, Asif Khan, and Pete Hodakievic. Embedded X86 Testing Methodology. In *Proceedings IEEE International Test Conference (ITC)*, pages 487–492, Atlantic City, NJ, USA, September 1999.
- [14] Subhayu Basu, Indranil Sengupta, Dipanwita Roy Chowdhury, and Sudipta Bhawmik. An Integrated Approach to Testing Embedded Cores and Interconnects Using Test Access Mechanism (TAM) Switch. *Journal of Electronic Testing: Theory and Applications*, 18(4/5):475–485, August 2002.
- [15] Subhayu Basu, Indranil Sengupta, Dipanwita Roy Chowdhury, and Sudipta Bhawmik. An Integrated Approach to Testing Embedded Cores and Interconnects Using Test Access Mechanism (TAM) Switch. In Krishnendu Chakrabarty, editor, *SOC (System-on-a-Chip) Testing for Plug and Play Test Automation*, volume 21 of *Frontiers in Electronics Testing*, pages 111–121. Kluwer Academic Publishers, September 2002.
- [16] Ken Batchter and Christos Papachristou. Instruction Randomization Self Test for Processor Cores. In *Proceedings IEEE VLSI Test Symposium (VTS)*, pages 34–40, Dana Point, CA, USA, April 1999.
- [17] Hakim Bederr and Franck Chirat. At-Speed Test of a DSP Subsystem Embeed in a Wireless Application Chip. In *Digest of Papers of IEEE International Workshop on Testing Embedded Core-Based Systems (TECS)*, pages 1.3–1–11, Dana Point, CA, USA, April 1999.
- [18] Frans Beenker. *Testability Concepts for Digital ICs*. PhD thesis, Twente University, Enschede, The Netherlands, April 1994.
- [19] Frans Beenker, Ben Bennetts, and Loek Thijssen. *Testability Concepts for Digital ICs - The Macro Test Approach*, volume 3 of *Frontiers in Electronics Testing*. Kluwer Academic Publishers, Boston, MA, USA, 1995.
- [20] Frans Beenker, Rob Dekker, Rudi Stans, and Max van der Star. A Testability Strategy for Silicon Compilers. In *Proceedings IEEE International Test Conference (ITC)*, pages 660–696, September 1989.
- [21] Frans Beenker, Rob Dekker, Rudi Stans, and Max van der Star. Implementing Macro Test in Silicon Compiler Designs. *IEEE Design & Test of Computers*, Vol. 7(No. 2):41–51, April 1990.
- [22] Frans Beenker, Karel van Eerdewijk, Robert Gerritsen, Frank Peacock, and Max van der Star. Macro Testing: Unifying IC and Board Test. *IEEE Design & Test of Computers*, Vol. 3(No. 4):26–32, December 1986.
- [23] M. Benabdenbi, A. Greiner, F. Pecheux, E. Viaud, and M. Tuna. STEPS: Experimenting a New Software-based Strategy for Testing SoCs Containing P1500-compliant IP Cores. In *Proceedings Design, Automation, and Test in Europe (DATE)*, pages 712–713, Paris, France, February 2004.

- [24] Mounir Benabdenbi, Walid Maroufi, and Meryem Marzouki. CAS-BUS: A Scalable and Reconfigurable Test Access Mechanism for Systems on a Chip. In *Proceedings Design, Automation, and Test in Europe (DATE)*, pages 141–145, Paris, France, March 2000.
- [25] Mounir Benabdenbi, Walid Maroufi, and Meryem Marzouki. Testing TAPed Cores and Wrapped Cores With The Same Test Access Mechanism. In *Proceedings Design, Automation, and Test in Europe (DATE)*, pages 150–155, Munich, Germany, March 2001.
- [26] Mounir Benabdenbi, Walid Maroufi, and Meryem Marzouki. CAS-BUS: A Test Access Mechanism and a Toolbox Environment for Core-Based System Chip Testing. *Journal of Electronic Testing: Theory and Applications*, 18(4/5):455–473, August 2002.
- [27] Mounir Benabdenbi, Walid Maroufi, and Meryem Marzouki. CAS-BUS: A Test Access Mechanism and a Toolbox Environment for Core-Based System Chip Testing. In Krishnendu Chakrabarty, editor, *SOC (System-on-a-Chip) Testing for Plug and Play Test Automation*, volume 21 of *Frontiers in Electronics Testing*, pages 91–109. Kluwer Academic Publishers, September 2002.
- [28] Ben Bennetts. A Design Strategy for System-on-a-Chip Testing. *Electronic Products*, pages 57–59, June 1997.
- [29] A. Benso, G. Borgonovo, D. Grassi, M. Lobetti-Bodoni, and A. Pricco. An Industrial Approach to Core Testing. In *Digest of Papers of IEEE International Workshop on Testing Embedded Core-Based Systems (TECS)*, pages 1.3–1–4, Washington, DC, USA, October 1998.
- [30] A. Benso, S. Chiusano, P. Prinetto, and Y. Zorian. HD-BIST: A Hierarchical Distributed BIST Architecture for System-on-a-Chip. In *Digest of Papers of IEEE International Workshop on Testing Embedded Core-Based Systems (TECS)*, pages 2.4–1–5, Washington, DC, USA, October 1998.
- [31] Alfredo Benso, Silvia Cataldo, Silvia Chiusano, Paolo Prinetto, and Yervant Zorian. A High-Level EDA Environment for the Automatic Insertion of HD-BIST Structures. In *Digest of Papers of IEEE International Workshop on Testing Embedded Core-Based Systems (TECS)*, pages 4.3–1–5, Dana Point, CA, USA, April 1999.
- [32] Alfredo Benso, Silvia Cataldo, Silvia Chiusano, Paolo Prinetto, and Yervant Zorian. HD-BIST: A Hierarchical Framework for BIST Scheduling and Diagnosis in SOCs. In *Proceedings IEEE International Test Conference (ITC)*, pages 1038–1044, Atlantic City, NJ, USA, September 1999.
- [33] Alfredo Benso et al. HD²BIST: A Hierarchical Framework for BIST Scheduling, Data Patterns Delivering and Diagnosis in SoCs. In *Digest of Papers of IEEE International Workshop on Testing Embedded Core-Based Systems (TECS)*, pages 3.3–1–8, Montreal, Canada, May 2000.
- [34] Alfredo Benso et al. HD²BIST: A Hierarchical Framework for BIST Scheduling, Data Patterns Delivering and Diagnosis in SoCs. In *Proceedings IEEE International Test Conference (ITC)*, pages 892–901, Atlantic City, NJ, USA, October 2000.
- [35] Sandeep Bhatia, Tushar Gheewala, and Prab Varma. A Unifying Methodology for Intellectual Property and Custom Logic Testing. In *Proceedings IEEE International Test Conference (ITC)*, pages 639–648, Washington, DC, USA, October 1996.
- [36] Debashis Bhattacharya. Hierarchical Test Access Architecture for Embedded Cores in an Integrated Circuit. In *Proceedings IEEE VLSI Test Symposium (VTS)*, pages 8–14, Monterey, CA, USA, April 1998.
- [37] Debashis Bhattacharya. Instruction-Driven Wake-Up Mechanisms for Snoopy TAP Controller. In *Proceedings IEEE VLSI Test Symposium (VTS)*, pages 467–472, Dana Point, CA, USA, April 1999.
- [38] A. Bommireddy, J. Khare, S. Shaikh, and S-T. Su. Test and Debug of Networking SoCs - A Case Study. In *Proceedings IEEE VLSI Test Symposium (VTS)*, pages 121–126, Montreal, Canada, April 2000.

- [39] Marcel Boosten and Harro Jacobs. Test Protocol Expansion: Memory Handling and Efficiency Improvements. Master's thesis, Eindhoven University of Technology, Eindhoven, The Netherlands, June 1994.
- [40] Frank Bouwman, Steven Oostdijk, Rudi Stans, Ben Bennetts, and Frans Beenker. Macro Testability; The Results of Production Device Applications. In *Proceedings IEEE International Test Conference (ITC)*, pages 232–241, September 1992.
- [41] Hans Bouwmeester. Reducing the Test Time of VLSI Devices by Exploiting Parallelism in Macro Test. Master's thesis, Delft University of Technology, Delft, The Netherlands, July 1992.
- [42] Hans Bouwmeester, Steven Oostdijk, Frank Bouwman, Rudi Stans, Loek Thijssen, and Frans Beenker. Minimizing Test Time by Exploiting Parallelism in Macro Test. In *Proceedings IEEE International Test Conference (ITC)*, pages 451–460, September 1993.
- [43] Andrew Burdass, Gary Campbell, Richard Grisenthwaite, and Richard York. Testing Embedded Synthesizable IP - A Case Study. In *Digest of Papers of IEEE International Workshop on Testing Embedded Core-Based Systems (TECS)*, pages 3.2–1–5, Montreal, Canada, May 2000.
- [44] Andrew Burdass et al. Embedded Test and Debug of Full Custom and Synthesizable Microprocessor Cores. In *Proceedings IEEE European Test Workshop (ETW)*, pages 17–22, Cascais, Portugal, May 2000.
- [45] Krishnendu Chakrabarty. Test Scheduling for Core-Based Systems. In *Proceedings International Conference on Computer-Aided Design (ICCAD)*, pages 391–394, San Jose, CA, USA, November 1999.
- [46] Krishnendu Chakrabarty. Design of System-on-a-Chip Test Access Architectures Under Place-and-Route and Power Constraints. In *Proceedings ACM/IEEE Design Automation Conference (DAC)*, pages 432–437, Los Angeles, CA, USA, June 2000.
- [47] Krishnendu Chakrabarty. Design of System-on-a-Chip Test Access Architectures Using Integer Linear Programming. In *Proceedings IEEE VLSI Test Symposium (VTS)*, pages 127–134, Montreal, Canada, April 2000.
- [48] Krishnendu Chakrabarty. Test Scheduling for Core-Based Systems Using Mixed-Integer Linear Programming. *IEEE Transactions on Computer-Aided Design*, 19(10):1163–1174, October 2000.
- [49] Krishnendu Chakrabarty. Optimal Test Access Architectures for System-on-a-Chip. *ACM Transactions on Design Automation of Electronic Systems*, 6(1):26–49, January 2001.
- [50] Krishnendu Chakrabarty and Erik Jan Marinissen. TECS'02 Panel Summary: How Useful Are The ITC'02 SOC Test Benchmarks? *IEEE Design & Test of Computers*, 19(5):119–120, September 2002.
- [51] Krishnendu Chakrabarty, Rajatish Mukherjee, and Andrew S. Exnicios. Synthesis of Transparent Circuits for Hierarchical and System-on-a-Chip Test. In *Proceedings IEEE International Conference on VLSI Design (ICVD)*, pages 431–436, Bangalore, India, January 2001.
- [52] Tapan J. Chakraborty, Sudipta Bhawmik, and Chen-Huan Chiang. Test Access Methodology for System-On-Chip Testing. In *Digest of Papers of IEEE International Workshop on Testing Embedded Core-Based Systems (TECS)*, pages 1.1–1–7, Montreal, Canada, May 2000.
- [53] Anshuman Chandra, Sharon Schweizer, Vikram Iyengar, and Krishnendu Chakrabarty. A Unified Approach for SOC Test Resource Partitioning Using Test Data Compression and TAM Optimization. In *Digest of Papers of IEEE International Workshop on Test Resource Partitioning (TRP)*, pages 4.4–1–7, Baltimore, MD, USA, October 2002.

- [54] R. Chandramouli and Stephen Pateras. Testing Systems on a Chip. *IEEE Spectrum*, pages 42–47, November 1996.
- [55] Li Chen et al. Embedded Hardware and Software Self-Testing Methodologies for Processor Cores. In *Proceedings ACM/IEEE Design Automation Conference (DAC)*, pages 625–630, Los Angeles, CA, USA, June 2000.
- [56] Kuo-Liang Cheng et al. An SOC Test Integration Platform and Its Industrial Realization. In *Proceedings IEEE International Test Conference (ITC)*, pages 1213–1222, Charlotte, NC, USA, October 2004.
- [57] James Chin and Mehrdad Nourani. SOC Test Scheduling With Power-Time Tradeoff and Hot Spot Avoidance. In *Proceedings Design, Automation, and Test in Europe (DATE)*, pages 710–711, Paris, France, February 2004.
- [58] Erika Cota, Luigi Carro, and Marcelo Lubaszewski. Reusing an On-Chip Network for the Test of Core-Based Systems. *ACM Transactions on Design Automation of Electronic Systems*, Vol. 9(No. 4):471–499, October 2004.
- [59] Érika Cota, Luigi Carro, Flávio Wagner, and Marcel Lubaszewski. Power-Aware NoC Reuse on the Testing of Core-Based Systems. In *Proceedings IEEE International Test Conference (ITC)*, pages 612–621, Charlotte, NC, USA, September 2003.
- [60] Érika Cota, Luigi Carro, Flávio Wagner, and Marcelo Lubaszewski. BISTed cores and Test Time Minimization in NOC-based Systems. In *Digest of Papers of IEEE International Workshop on Test Resource Partitioning (TRP)*, pages 1–6, Napa, CA, USA, April 2003.
- [61] Érika Cota, Luigi Carro, Flávio Wagner, and Marcelo Lubaszewski. Power-Aware NoC Reuse on the Testing of Core-Based Systems. In *Digest of Papers of IEEE European Test Workshop (ETW)*, pages 123–128, Maastricht, The Netherlands, May 2003.
- [62] Érika Cota et al. The Impact of NoC Reuse on the Testing of Core-based Systems. In *Proceedings IEEE VLSI Test Symposium (VTS)*, pages 128–133, Napa, CA, USA, April 2003.
- [63] Al Crouch and Jeff Freeman. ColdFire Processor is Hot for DfT. *Test - The European Test Industry Journal*, Vol. 24(No. 6):15–16, July 1998.
- [64] Francisco DaSilva, editor. *IEEE Std 1500TM-2005, IEEE Standard Testability Method for Embedded Core-based Integrated Circuits*. IEEE, New York, NY, USA, August 2005.
- [65] Francisco DaSilva, Yervant Zorian, Lee Whetsel, Karim Arabi, and Rohit Kapur. Overview of the IEEE P1500 Standard. In *Proceedings IEEE International Test Conference (ITC)*, pages 988–997, Charlotte, NC, USA, September 2003.
- [66] Hiroshi Date, Toshinori Hosokawa, and Michiaki Muraoka. A SoC Test Strategy Based on a Non-Scan DFT Method. In *Proceedings IEEE Asian Test Symposium (ATS)*, pages 305–310, Tamuning, Guam, USA, November 2002.
- [67] Kaushik De. Test Methodology for Embedded Cores which Protects Intellectual Property. In *Proceedings IEEE VLSI Test Symposium (VTS)*, pages 2–9, Monterey, CA, USA, April 1997.
- [68] Bulent Dervisoglu. Designing Hierarchical Test Access Controllers for Embedded Cores using IEEE P1500 and VSIA Compliant Architectures. In *Digest of Papers of IEEE European Test Workshop (ETW)*, pages 101–106, Saltsjobaden, Sweden, May 2001.
- [69] Bulent Dervisoglu and Janardhana Swamy. A Novel Approach for Designing a Hierarchical Test Access Controller for Embedded Core Designs in an SoC Environment. In *Digest of Papers of IEEE International Workshop on Testing Embedded Core-Based Systems (TECS)*, pages 1.4–1–7, Montreal, Canada, May 2000.

- [70] Sujit Dey, Erik Jan Marinissen, and Yervant Zorian. Testing System Chips: Methodologies and Experiences. *Integrated System Design*, Vol. 11(No. 123):36–48, September 1999.
- [71] O.P. Dias, J. Semiao, I.M. Teixeira, and J.P. Teixeira. Soft Wrapper Design for Embedded Cores Using a System Level Approach. In *Digest of Papers of IEEE International Workshop on Testing Embedded Core-Based Systems (TECS)*, pages 4.4–1–7, Dana Point, CA, USA, April 1999.
- [72] Rainer Dorsch, Ramon Huerta Rivera, Hans-Joachim Wunderlich, and Martin Fischer. Adapting an SoC to ATE Concurrent Test Capabilities. In *Proceedings IEEE International Test Conference (ITC)*, pages 1169–1175, Baltimore, MD, USA, October 2002.
- [73] Frank S. Eory. A Core-Based System-to-Silicon Design Methodology. *IEEE Design & Test of Computers*, 14(4):36–41, December 1997.
- [74] T. Falter and D. Richter. Overview of Status and Challenges of System Testing on Chip with Embedded DRAMs. *Solid State Electronics*, 44(5):761, 2000.
- [75] Chris Feige, Jan ten Pierick, Clemens Wouters, Ronald Tangelder, and Hans Kerkhoff. Integration of the Scan-Test Method into an Architecture Specific Core-Test Approach. In *Digest of Papers of IEEE European Test Workshop (ETW)*, Barcelona, Spain, May 1998.
- [76] Chris Feige, Jan ten Pierick, Clemens Wouters, Ronald Tangelder, and Hans G. Kerkhoff. Integration of the Scan-Test Method into an Architecture Specific Core-Test Approach. *Journal of Electronic Testing: Theory and Applications*, 14(1–2):125–131, February 1999.
- [77] Chris Feige and Clemens Wouters. Integration of Structural Test Methods into a Architecture Specific Core-Test Approach. In *Digest of Papers of IEEE International Workshop on Testing Embedded Core-Based Systems (TECS)*, pages 5.2–1–8, Washington, DC, USA, October 1998.
- [78] Fabrizio Ferrandi et al. Testing Core-Based Systems: A Symbolic Methodology. *IEEE Design & Test of Computers*, 14(4):69–77, December 1997.
- [79] Martin Fischer, Ramon Huerta Rivera, Rainer Dorsch, and Hans-Joachim Wunderlich. Adapting an SoC to ATE Concurrent Test Capabilities. In *Digest of Papers of IEEE European Test Workshop (ETW)*, pages 275–280, Corfu, Greece, May 2002.
- [80] Marie-Lise Flottes, Julien Pouget, and Bruno Rouzeyre. Sessionless Test Scheme: Power-Constrained Test Scheduling for System-on-a-Chip. In *Proceedings IFIP International Conference on Very Large Scale Integration (VLSI-SOC)*, pages 105–110, Montpellier, France, December 2001.
- [81] Marie-Lise Flottes, Julien Pouget, and Bruno Rouzeyre. Power-Constrained Test Scheduling for SOCs Under a “No Session” Scheme. In Michel Robert, Bruno Rouzeyre, Christian Pigué, and Marie-Lise Flottes, editors, *SOC Design Methodologies*, pages 401–412. Kluwer Academic Publishers, 2002.
- [82] Patrick Gallagher et al. A Building Block BIST Methodology for SOC Designs: A Case Study. In *Proceedings IEEE International Test Conference (ITC)*, pages 111–120, Baltimore, MD, USA, October 2001.
- [83] Indradeep Ghosh, Sujit Dey, and Niraj K. Jha. A Fast and Low Cost Testing Technique for Core-based System-on-Chip. In *Proceedings ACM/IEEE Design Automation Conference (DAC)*, pages 542–547, San Francisco, CA, USA, June 1998. Association for Computing Machinery, Inc.
- [84] Indradeep Ghosh, Sujit Dey, and Niraj K. Jha. A Fast and Low-Cost Testing Technique for Core-Based System-Chips. *IEEE Transactions on Computer-Aided Design*, 19(8):863, August 2000.
- [85] Indradeep Ghosh, Niraj K. Jha, and Sujit Dey. A Low Overhead Design for Testability and Test Generation Technique for Core-Based Systems. In *Proceedings IEEE International Test Conference (ITC)*, pages 50–59, Washington, DC, USA, November 1997.

- [86] Indradeep Ghosh, Niraj K. Jha, and Sujit Dey. Low Overhead Design for Testability and Test Generation Technique for Core-Based Systems-on-a-Chip. *IEEE Transactions on Computer-Aided Design*, 18(11):1661, November 1999.
- [87] Sandeep Kumar Goel. Test Access Planning for Embedded Core-Based System ICs. Master's thesis, Indian Institute of Technology Delhi, New Delhi, India, December 1999.
- [88] Sandeep Kumar Goel. A Novel Wrapper Cell Design for Efficient Testing of Hierarchical Cores in System Chips. In *Digest of Papers of IEEE European Test Symposium (ETS)*, pages 147–152, Ajaccio, Corsica, France, May 2004.
- [89] Sandeep Kumar Goel, Kuoshu Chiu, Erik Jan Marinissen, Toan Nguyen, and Steven Oostdijk. Test Infrastructure Design for the NexperiaTM Home Platform PNX8550 System Chip. In *Proceedings Design, Automation, and Test in Europe (DATE) Designers Forum*, pages 108–113, Paris, France, February 2004.
- [90] Sandeep Kumar Goel and Erik Jan Marinissen. TAM Architectures and Their Implication on Test Application Time. In *Digest of Papers of IEEE International Workshop on Testing Embedded Core-Based Systems (TECS)*, pages 3.3–1–10, Marina del Rey, CA, USA, May 2001.
- [91] Sandeep Kumar Goel and Erik Jan Marinissen. A Novel Test Time Reduction Algorithm for Test Architecture Design for Core-Based System Chips. In *Proceedings IEEE European Test Workshop (ETW)*, pages 7–12, Corfu, Greece, May 2002.
- [92] Sandeep Kumar Goel and Erik Jan Marinissen. Cluster-Based Test Architecture Design for System-on-Chip. In *Proceedings IEEE VLSI Test Symposium (VTS)*, pages 259–264, Monterey, CA, USA, April 2002.
- [93] Sandeep Kumar Goel and Erik Jan Marinissen. Effective and Efficient Test Architecture Design for SOCs. In *Proceedings IEEE International Test Conference (ITC)*, pages 529–538, Baltimore, MD, USA, October 2002.
- [94] Sandeep Kumar Goel and Erik Jan Marinissen. A Test Time Reduction Algorithm for Test Architecture Design for Core-Based System Chips. *Journal of Electronic Testing: Theory and Applications*, 19(4):425–435, August 2003.
- [95] Sandeep Kumar Goel and Erik Jan Marinissen. Control-Aware Test Architecture Design for Modular SOC Testing. In *Proceedings IEEE European Test Workshop (ETW)*, pages 57–62, Maastricht, The Netherlands, May 2003.
- [96] Sandeep Kumar Goel and Erik Jan Marinissen. Layout-Driven SOC Test Architecture Design for Test Time and Wire Length Minimization. In *Proceedings Design, Automation, and Test in Europe (DATE)*, pages 738–743, Munich, Germany, March 2003.
- [97] Sandeep Kumar Goel and Erik Jan Marinissen. SOC Test Architecture Design for Efficient Utilization of Test Bandwidth. *ACM Transactions on Design Automation of Electronic Systems*, 8(4):399–429, October 2003.
- [98] Sandeep Kumar Goel and Erik Jan Marinissen. On-Chip Test Infrastructure Design for High-Throughput Multi-Site Testing of SOCs. In *Digest of Papers of IEEE International Infrastructure IP Workshop (IIP)*, page 1.1, Charlotte, NC, USA, 2004.
- [99] Sandeep Kumar Goel and Erik Jan Marinissen. TR-Architect: DfT and Test Support for SOC Designers. In *Proceedings of the IEEE/ProRISC Symposium on Circuits, Systems and Signal Processing*, Veldhoven, The Netherlands, November 2004.
- [100] Sandeep Kumar Goel and Erik Jan Marinissen. On-Chip Test Infrastructure Design for Optimal Multi-Site Testing of System Chips. In *Proceedings Design, Automation, and Test in Europe (DATE)*, pages 44–49, Munich, Germany, March 2005.

- [101] M. Goessel, E.S. Sogomonyan, and A. Morosov. A New Totally Error Propagating Compactor for Arbitrary Cores With Digital Interfaces. In *Proceedings IEEE VLSI Test Symposium (VTS)*, pages 49–56, Dana Point, CA, USA, April 1999.
- [102] Paul T. Gonciari, Bashir M. Al-Hashimi, and Nicola Nicolici. Integrated Test Data Decompression and Core Wrapper Design for Low-Cost System-on-a-Chip Testing. In *Proceedings IEEE International Test Conference (ITC)*, pages 64–73, Baltimore, MD, USA, October 2002.
- [103] Paul T. Gonciari, Bashir M. Al-Hashimi, and Nicola Nicolici. Useless Memory Allocation in System-on-a-Chip Test: Problems and Solutions. In *Proceedings IEEE VLSI Test Symposium (VTS)*, pages 423–429, Monterey, CA, USA, April 2002.
- [104] Liam Goudge. Debugging Embedded Systems. <http://www.arm.com/Documentation/WhitePapers/DebugEmbSys>, 1998.
- [105] Bruce S. Greene and Samiha Mourad. Accessing Cores through Scan Path Chains. In *Digest of Papers of IEEE International Workshop on Testing Embedded Core-Based Systems (TECS)*, pages 4.2–1–4, Dana Point, CA, USA, April 1999.
- [106] Kevin M. Grosselfinger and James A. Monzel. A Production Test Environment for Complex System On a Chip ASIC Products Incorporating the Rambus ASIC Cell. In *Digest of Papers of IEEE International Workshop on Testing Embedded Core-Based Systems (TECS)*, pages 3.3–1–6, Washington, DC, USA, October 1998.
- [107] Rajesh K. Gupta and Yervant Zorian. Introducing Core-Based System Design. *IEEE Design & Test of Computers*, 14(4):15–25, December 1997.
- [108] Alan Hales and Erik Jan Marinissen. IEEE P1500 Web Site. <http://grouper.ieee.org/groups/1500/>.
- [109] Peter Harrod. Testing Reusable IP - A Case Study. In *Proceedings IEEE International Test Conference (ITC)*, pages 493–498, Atlantic City, NJ, USA, September 1999.
- [110] Shankar Hemmady, Tom Anderson, and Yervant Zorian. Verification and Testing of Embedded Cores. In *Proceedings of Design SuperCon*, pages S122–1–19, January 1997.
- [111] Mohammad Hosseinabady, Abbas Banaiyan, Mahdi Nazm Bojnordi, and Zainalabedin Navabi. A Concurrent Testing Method for NoC Switches. In *Proceedings Design, Automation, and Test in Europe (DATE)*, pages 1–6, Munich, Germany, March 2006.
- [112] Huan-Shan Hsu et al. Test Scheduling and Test Access Architecture Optimization for System-on-Chip. In *Proceedings IEEE Asian Test Symposium (ATS)*, pages 411–416, Tamuning, Guam, USA, November 2002.
- [113] Jing-Reng Huang, Madhu K. Iyer, and Kwang-Ting Cheng. A Self-Test Methodology for IP Cores in Bus-Based Programmable SOCs. In *Proceedings IEEE VLSI Test Symposium (VTS)*, pages 198–203, Marina del Rey, CA, USA, May 2001.
- [114] Yu Huang et al. Resource Allocation and Test Scheduling for Concurrent Test of Core-Based SOC Design. In *Proceedings IEEE Asian Test Symposium (ATS)*, pages 265–270, Kyoto, Japan, November 2001.
- [115] Yu Huang et al. Constraint-Driven Pin Mapping for Concurrent SOC Testing. In *Proceedings IEEE Asia South Pacific Design Automation Conference (ASP-DAC)*, Bangalore, India, January 2002.
- [116] Yu Huang et al. On Concurrent Test of Core-Based SOC Design. *Journal of Electronic Testing: Theory and Applications*, 18(4/5):401–414, August 2002.
- [117] Yu Huang et al. On Concurrent Test of Core-Based SOC Design. In Krishnendu Chakrabarty, editor, *SOC (System-on-a-Chip) Testing for Plug and Play Test Automation*, volume 21 of *Frontiers in Electronics Testing*, pages 37–50. Kluwer Academic Publishers, September 2002.

- [118] Yu Huang et al. Optimal Core Wrapper Width Selection and SOC Test Scheduling Based on 3-D Bin Packing Algorithm. In *Digest of Papers of IEEE European Test Workshop (ETW)*, pages 35–40, Corfu, Greece, May 2002.
- [119] Yu Huang et al. Optimal Core Wrapper Width Selection and SOC Test Scheduling Based on 3-D Bin Packing Algorithm. In *Proceedings IEEE International Test Conference (ITC)*, pages 74–82, Baltimore, MD, USA, October 2002.
- [120] Yu Huang, Sudhakar M. Reddy, and Wu-Tung Cheng. Core-Clustering Based SOC Test Scheduling Optimization. In *Proceedings IEEE Asian Test Symposium (ATS)*, pages 405–410, Tamuning, Guam, USA, November 2002.
- [121] Paul Hughes, Peter Harrod, and Gary Campbell. Embedded CPU Test Strategies. In *Digest of Papers of IEEE European Test Workshop (ETW)*, pages 281–285, Corfu, Greece, May 2002.
- [122] Merrill Hunt and James A. Rowson. Blocking in a System on a Chip. *IEEE Spectrum*, pages 35–41, November 1996.
- [123] Sungbae Hwang and Jacob A. Abraham. Microprocessor Based Test Structure for SOC. In *Digest of Papers of IEEE International Workshop on Testing Embedded Core-Based Systems (TECS)*, pages 4.3–1–7, Marina del Rey, CA, USA, May 2001.
- [124] Sungbae Hwang and Jacob A. Abraham. Reuse of Addressable System Bus for SOC Testing. In *Proceedings IEEE International ASIC/SOC Conference*, pages 215–219, Washington, DC, USA, September 2001.
- [125] Venkata Immaneni and Srinivas Raman. Direct Access Test Scheme - Design of Block and Core Cells for Embedded ASICs. In *Proceedings IEEE International Test Conference (ITC)*, pages 488–492, September 1990.
- [126] Urban Ingelsson, Sandeep Kumar Goel, Erik Larsson, and Erik Jan Marinissen. Test Scheduling for Modular SOCs in an Abort-on-Fail Environment. In *Proceedings IEEE European Test Symposium (ETS)*, pages 8–13, Tallinn, Estonia, May 2005.
- [127] Vikram Iyengar and Krishnendu Chakrabarty. Co-Optimization of Test Wrapper and Test Access Architecture for Embedded Cores. In *Digest of Papers of IEEE European Test Workshop (ETW)*, pages 189–194, Saltsjobaden, Sweden, May 2001.
- [128] Vikram Iyengar and Krishnendu Chakrabarty. Iterative Test Wrapper and Test Access Mechanism Co-Optimization. In *Digest of Papers of IEEE International Workshop on Testing Embedded Core-Based Systems (TECS)*, pages 1.4–1–7, Marina del Rey, CA, USA, May 2001.
- [129] Vikram Iyengar and Krishnendu Chakrabarty. Precedence-Based, Preemptive, and Power-Constrained Test Scheduling for System-on-a-Chip. In *Proceedings IEEE VLSI Test Symposium (VTS)*, pages 368–374, Marina del Rey, CA, USA, May 2001.
- [130] Vikram Iyengar and Krishnendu Chakrabarty. Test Bus Sizing for System-on-a-Chip. *IEEE Transactions on Computers*, 51:449–459, May 2002.
- [131] Vikram Iyengar, Krishnendu Chakrabarty, Mark D. Krasniewski, and Gopind N. Kumar. Design and Optimization of Multi-level TAM Architectures for Hierarchical SOCs. In *Proceedings IEEE VLSI Test Symposium (VTS)*, pages 299–304, Napa, CA, USA, April 2003.
- [132] Vikram Iyengar, Krishnendu Chakrabarty, and Erik Jan Marinissen. Test Wrapper and Test Access Mechanism Co-Optimization for System-on-Chip. In *Proceedings IEEE International Test Conference (ITC)*, pages 1023–1032, Baltimore, MD, USA, October 2001.
- [133] Vikram Iyengar, Krishnendu Chakrabarty, and Erik Jan Marinissen. Co-Optimization of Test Wrapper and Test Access Architecture for Embedded Cores. *Journal of Electronic Testing: Theory and Applications*, 18(2):213–230, April 2002.

- [134] Vikram Iyengar, Krishnendu Chakrabarty, and Erik Jan Marinissen. Efficient Wrapper/TAM Co-Optimization for Large SOCs. In *Proceedings Design, Automation, and Test in Europe (DATE)*, pages 491–498, Paris, France, March 2002.
- [135] Vikram Iyengar, Krishnendu Chakrabarty, and Erik Jan Marinissen. Integrated Wrapper/TAM Co-Optimization, Constraint-Driven Test Scheduling, and Tester Data Volume Reduction for SOCs. In *Proceedings ACM/IEEE Design Automation Conference (DAC)*, pages 685–690, New Orleans, LO, USA, June 2002.
- [136] Vikram Iyengar, Krishnendu Chakrabarty, and Erik Jan Marinissen. On Using Rectangle Packing for SOC Wrapper/TAM Co-Optimization. In *Proceedings IEEE VLSI Test Symposium (VTS)*, pages 253–258, Monterey, CA, USA, April 2002.
- [137] Vikram Iyengar, Krishnendu Chakrabarty, and Erik Jan Marinissen. Recent Advances in Test Planning for Modular Testing of Core-Based SOCs. In *Proceedings IEEE Asian Test Symposium (ATS)*, pages 320–325, Tamuning, Guam, USA, November 2002.
- [138] Vikram Iyengar, Krishnendu Chakrabarty, and Erik Jan Marinissen. Test Resource Optimization for Multi-Site Testing of Embedded-Core-Based SOCs Using ATE With Memory Depth Constraints. In *Digest of Papers of IEEE European Test Workshop (ETW)*, pages 29–34, Corfu, Greece, May 2002.
- [139] Vikram Iyengar, Krishnendu Chakrabarty, and Erik Jan Marinissen. Efficient Test Access Mechanism Optimization for System-on-Chip. *IEEE Transactions on Computer-Aided Design*, 22(5):635–643, May 2003.
- [140] Vikram Iyengar, Krishnendu Chakrabarty, and Erik Jan Marinissen. Test Access Mechanism Optimization, Test Scheduling and Tester Data Volume Reduction for System-on-Chip. *IEEE Transactions on Computers*, 52(12):1619–1632, December 2003.
- [141] Vikram Iyengar, Anshuman Chandra, Sharon Schweizer, and Krishnendu Chakrabarty. A Unified Approach for SOC Testing Using Test Data Compression and TAM Optimization. In *Proceedings Design, Automation, and Test in Europe (DATE)*, pages 1188–1189, Munich, Germany, March 2003.
- [142] Vikram Iyengar, Sandeep Kumar Goel, Krishnendu Chakrabarty, and Erik Jan Marinissen. Test Resource Optimization for Multi-Site Testing of SOCs Under ATE Memory Depth Constraints. In *Proceedings IEEE International Test Conference (ITC)*, pages 1159–1168, Baltimore, MD, USA, October 2002.
- [143] Vikram Iyengar, Sandeep Kumar Goel, Erik Jan Marinissen, and Krishnendu Chakrabarty. On SOC Test Resource Optimization for Multi-Site Testing Using ATE With Memory Depth Constraints. In *Proceedings North-American Test Workshop (NATW)*, pages 77–83, Montauk, NY, USA, May 2002.
- [144] Vikram Iyengar, Makoto Sugihara, Hiroshi Date, and Krishnendu Chakrabarty. Intellectual Property Protection Using Partially-Mergeable Cores. In *Digest of Papers of IEEE International Workshop on Testing Embedded Core-Based Systems (TECS)*, pages 4.3–1–7, Montreal, Canada, May 2000.
- [145] Abhijit Jas, Bahram Pouya, and Nur Touba. Scan Length Reduction in Cores Using Virtual Scan Chains. In *Digest of Papers of IEEE International Workshop on Testing Embedded Core-Based Systems (TECS)*, pages 4.1–1–6, Dana Point, CA, USA, April 1999.
- [146] Abhijit Jas, Bahram Pouya, and Nur Touba. Virtual Scan Chains: A Means for Reducing Scan Length in Cores. In *Proceedings IEEE VLSI Test Symposium (VTS)*, pages 73–78, Montreal, Canada, April 2000.
- [147] Abhijit Jas and Nur Touba. Test Vector Decompression Via Cyclical Scan Chains and Its Application to Testing Core-Based Designs. In *Proceedings IEEE International Test Conference (ITC)*, pages 458–464, Washington, DC, USA, October 1998.

- [148] Abhijit Jas and Nur Touba. Using an Embedded Processor for Efficient Deterministic Testing of Systems-on-a-Chip. In *Proceedings International Conference on Computer Design (ICCD)*, Austin, TX, USA, October 1999.
- [149] Rohit Kapur et al. P1500-CTL: Towards a Standard Core Test Language. In *Proceedings IEEE VLSI Test Symposium (VTS)*, pages 489–490, Dana Point, CA, USA, April 1999.
- [150] Rohit Kapur et al. CTL – The Language for Describing Core-Based Test. In *Proceedings IEEE International Test Conference (ITC)*, pages 131–139, Baltimore, MD, USA, October 2001.
- [151] Rohit Kapur and Tom W. Williams. Manufacturing Test of SoCs. In *Proceedings IEEE Asian Test Symposium (ATS)*, pages 317–319, Tamuning, Guam, USA, November 2002.
- [152] Jake Karrfalt, Zainalabedin Navabi, and Casper Stoel. A Novel Approach to Optimization IEEE 1149.1 for Systems with Multiple Embedded Cores. In *Digest of Papers of IEEE International Workshop on Testing Embedded Core-Based Systems (TECS)*, pages 2.2–1–10, Washington, DC, USA, October 1998.
- [153] Michael Kessler et al. Using a Hierarchical DFT Methodology in High Frequency Processor Designs for Improved Delay Fault Testability. In *Proceedings IEEE International Test Conference (ITC)*, pages 461–469, Baltimore, MD, USA, October 2001.
- [154] Michael Kessler, Gundolf Kiefer, Jens Leenstra, Kunt Schuenemann, Thomas Schwarz, and Hans-Joachim Wunderlich. Using a Hierarchical DFT Methodology in High Frequency Processor Designs for Improved Delay Fault Testability. In *Digest of Papers of IEEE European Test Workshop (ETW)*, pages 237–241, Saltsjobaden, Sweden, May 2001.
- [155] Hyungwon Kim and John P. Hayes. High-Coverage ATPG for Datapath Circuits with Unimplemented Blocks. In *Proceedings IEEE International Test Conference (ITC)*, pages 577–586, Washington, DC, USA, October 1998.
- [156] Hyungwon Kim and John P. Hayes. Realization-Independent Testing of IP-Based Systems. In *IEEE Fault-Tolerant Computing Symposium (FTCS)*, 1998.
- [157] Hyungwon Kim and John P. Hayes. Delay Fault Testing of Designs with Embedded IP Cores. In *Proceedings IEEE VLSI Test Symposium (VTS)*, pages 160–167, Dana Point, CA, USA, April 1999.
- [158] Hyungwon Kim and John P. Hayes. Delay Fault Testing of IP-Based Designs Via Symbolic Path Modeling. In *Proceedings IEEE International Test Conference (ITC)*, pages 1045–1054, Atlantic City, NJ, USA, September 1999.
- [159] Hyungwon Kim and John P. Hayes. On-Line Delay Fault Testing of IP-Based Systems Via Selectively Transparent Scan. In *Proceedings IEEE International On-Line Testing Workshop (IOLTW)*, Rhodos, Greece, July 1999.
- [160] Jong-Sun Kim et al. On-Chip Network Based Embedded Core Testing. In *Proceedings IEEE International SOC Conference (SOCC)*, pages 223–226, Santa Clara, CA, USA, September 2004.
- [161] K.Y. Ko, Mike W.T. Wong, and Y.S. Lee. Testing System-On-Chip by Summation of Cores’ Test Output Voltages. In *Proceedings IEEE Asian Test Symposium (ATS)*, pages 350–355, Tamuning, Guam, USA, November 2002.
- [162] Bernd Koenemann and Ken Wagner. Test Sockets: A Test Framework for System-On-Chip Designs. <http://grouper.ieee.org/groups/1500/pastmeetings.html#970427>, April 1997. Presentation at IEEE P1500 Working Group Meeting, Monterey, CA, April 1997.
- [163] Sandeep Koranne. On Test Planning for Core-Based SOCs. In *Proceedings of ECCO XIV*, May 2001.

- [164] Sandeep Koranne. A Novel Reconfigurable Wrapper for Testing of Embedded Core-Based SOCs and its Associated Scheduling Algorithm. *Journal of Electronic Testing: Theory and Applications*, 18(4/5):415–434, August 2002.
- [165] Sandeep Koranne. A Novel Reconfigurable Wrapper for Testing of Embedded Core-Based SOCs and its Associated Scheduling Algorithm. In Krishnendu Chakrabarty, editor, *SOC (System-on-a-Chip) Testing for Plug and Play Test Automation*, volume 21 of *Frontiers in Electronics Testing*, pages 51–70. Kluwer Academic Publishers, September 2002.
- [166] Sandeep Koranne. A Novel Test Access Wrapper Design for Embedded Cores. In *IEEE International Test Synthesis Workshop (ITSW)*, Santa Barbara, CA, USA, March 2002.
- [167] Sandeep Koranne. Design of Reconfigurable Core Wrappers for Embedded Core Based SOC Test. In *Proceedings International Symposium on Quality of Electronic Design (ISQED)*, San Jose, CA, USA, March 2002.
- [168] Sandeep Koranne. Formulating SoC Test Scheduling as a Network Transportation Problem. *IEEE Transactions on Computer-Aided Design*, 21(12):1517–1525, December 2002.
- [169] Sandeep Koranne. On Test Scheduling for Core-Based SOCs. In *Proceedings International Conference on VLSI Design*, pages 505–510, Bangalore, India, January 2002.
- [170] Sandeep Koranne. Test Resource Partitioning and Scheduling Using Graph Factoring. In *Digest of Papers of IEEE International Workshop on Test Resource Partitioning (TRP)*, pages 3.1–1–8, Baltimore, MD, USA, October 2002.
- [171] Sandeep Koranne. Solving the SoC Test Scheduling Problem Using Network Flow and Reconfigurable Wrappers. In *Proceedings International Symposium on Quality of Electronic Design (ISQED)*, pages 93–98, San Jose, CA, USA, March 2003.
- [172] Sandeep Koranne and Vishal Choudhary. Formulating SOC Test Scheduling as a Network Transportation Problem. In *Proceedings Design, Automation, and Test in Europe (DATE)*, Paris, France, March 2002.
- [173] Sandeep Koranne and Vikram Iyengar. On the Use of k-tuples for SoC Test Schedule Representation. In *Proceedings IEEE International Test Conference (ITC)*, pages 539–548, Baltimore, MD, USA, October 2002.
- [174] Ludovic Krundel, Sandeep Kumar Goel, Erik Jan Marinissen, Marie-Lise Flottes, and Bruno Rouzeyre. User-Constrained Test Architecture Design for Modular SOC Testing. In *Proceedings IEEE European Test Symposium (ETS)*, pages 80–85, Ajaccio, Corsica, France, May 2004.
- [175] Erik Larsson. *An Integrated System-Level Design for Testability Methodology*. PhD thesis, Linköpings Universitet, Linköping, Sweden, November 2000.
- [176] Erik Larsson. Integrating Core Selection in the SOC Test Solution Design-Flow. In *Proceedings IEEE International Test Conference (ITC)*, pages 1349–1358, Charlotte, NC, USA, October 2004.
- [177] Erik Larsson, Klas Arvidsson, Hideo Fujiwara, and Zebo Peng. Integrated Test Scheduling, Test Parallelization and TAM Design. In *Proceedings IEEE Asian Test Symposium (ATS)*, pages 397–404, Tamuning, Guam, USA, November 2002.
- [178] Erik Larsson and Hideo Fujiwara. Power Constrained Preemptive TAM Scheduling. In *Proceedings IEEE European Test Workshop (ETW)*, pages 119–126, Corfu, Greece, May 2002.
- [179] Erik Larsson and Hideo Fujiwara. Test Resource Partitioning and Optimization for SOC Designs. In *Proceedings IEEE VLSI Test Symposium (VTS)*, pages 319–324, Napa, CA, USA, April 2003.
- [180] Erik Larsson and Zebo Peng. Power-Aware Test Planning in the Early System-On-Chip Design Exploration Process. *IEEE Transactions on Computers*, 6(2):227–239, February 1996.

- [181] Erik Larsson and Zebo Peng. An Integrated System-on-Chip Test Framework. In *Proceedings Design, Automation, and Test in Europe (DATE)*, pages 138–144, Munich, Germany, March 2001.
- [182] Erik Larsson and Zebo Peng. System-on-Chip Test Parallelization under Power Constraints. In *Digest of Papers of IEEE European Test Workshop (ETW)*, pages 281–283, Saltsjobaden, Sweden, May 2001.
- [183] Erik Larsson and Zebo Peng. Test Scheduling and Scan-Chain Division Under Power Constraint. In *Proceedings IEEE Asian Test Symposium (ATS)*, pages 259–264, Kyoto, Japan, November 2001.
- [184] Erik Larsson and Zebo Peng. An Integrated Framework for the Design and Optimization of SOC Test Solutions. *Journal of Electronic Testing: Theory and Applications*, 18(4/5):385–400, August 2002.
- [185] Erik Larsson and Zebo Peng. An Integrated Framework for the Design and Optimization of SOC Test Solutions. In Krishnendu Chakrabarty, editor, *SOC (System-on-a-Chip) Testing for Plug and Play Test Automation*, volume 21 of *Frontiers in Electronics Testing*, pages 21–36. Kluwer Academic Publishers, September 2002.
- [186] Erik Larsson and Zebo Peng. A Reconfigurable Power-Conscious Core Wrapper and its Application to SOC Test Scheduling. In *Proceedings IEEE International Test Conference (ITC)*, pages 1135–1144, Charlotte, NC, USA, September 2003.
- [187] Erik Larsson, Zebo Peng, and Gunnar Carlsson. The Design and Optimization of SOC Test Solutions. In *Proceedings International Conference on Computer-Aided Design (ICCAD)*, pages 523–530, San Jose, CA, USA, November 2001.
- [188] Jim Lipman. The Hard Facts about Soft Cores. *EDN*, page 35, September 1996.
- [189] Jim Lipman. Add Testability Now to Core-Based Chips, or Pay Later. *EDN*, 43(4):65–78, February 1998.
- [190] Chunsheng Liu and Krishnendu Chakrabarty. A Partition-Based Approach for Identifying Failing Scan Cells in Scan-BIST with Applications to System-on-Chip Fault Diagnosis. In *Proceedings Design, Automation, and Test in Europe (DATE)*, pages 230–235, Munich, Germany, March 2003.
- [191] Chunsheng Liu, Erika Cota, Hamid Sharif, and D.K. Pradhan. Test Scheduling for Network-on-Chip with BIST and Precedence Constraints. In *Proceedings IEEE International Test Conference (ITC)*, pages 1369–1378, Charlotte, NC, USA, October 2004.
- [192] Chunsheng Liu and Vikram Iyengar. Test Scheduling with Thermal Optimization for Network-on-Chip Systems Using Variable-Rate On-Chip Clocking. In *Proceedings Design, Automation, and Test in Europe (DATE)*, pages 1–6, Munich, Germany, March 2006.
- [193] Chunsheng Liu, Vikram Iyengar, and D.K. Pradhan. Thermal-Aware Testing of Network-on-Chip Using Multiple-Frequency Clocking. In *Proceedings IEEE VLSI Test Symposium (VTS)*, pages 46–51, Berkeley, CA, USA, May 2006.
- [194] Chunsheng Liu, Zach Link, and D.K. Pradhan. Reuse-Based Test Access and Integrated Test Scheduling for Network-on-Chip. In *Proceedings Design, Automation, and Test in Europe (DATE)*, pages 1–6, Munich, Germany, March 2006.
- [195] Chunsheng Liu, Jiangfan Shi, Erika Cota, and Vikram Iyengar. Power-Aware Test Scheduling in Network-on-Chip Using Variable-Rate On-Chip Clocking. In *Proceedings IEEE VLSI Test Symposium (VTS)*, pages 349–354, Palm Springs, CA, USA, May 2005.
- [196] Samy Makar. Strategies for Testing Embedded Cores at Cirrus Logic. In *Digest of Papers of IEEE International Workshop on Testing Embedded Core-Based Systems (TECS)*, pages 1.2–1–5, Dana Point, CA, USA, April 1999.

- [197] Samy Makar. Beyond the Standard. In *Digest of Papers of IEEE International Workshop on Test Resource Partitioning (TRP)*, pages 1–7, Napa, CA, USA, April 2003.
- [198] Yiorgos Makris, Vishal Patel, and Alex Orailoglu. Efficient Transparency Extraction and Utilization in Hierarchical Test. In *Proceedings IEEE VLSI Test Symposium (VTS)*, pages 246–251, Marina del Rey, CA, USA, May 2001.
- [199] Erik Jan Marinissen. The TECS Bibliography Homepage. <http://www.extra.research.philips.com/itc02socbenchm/bib/>.
- [200] Erik Jan Marinissen. The TECS Bibliography (BIB_T_E_X) database file `tecs.bib`. <http://www.extra.research.philips.com/itc02socbenchm/bib/tecs.bib.gz>.
- [201] Erik Jan Marinissen. Philips' Approach to Core-Based System Chip Testing. In *Proceedings IEEE Design and Diagnostics of Electronic Circuits and Systems Workshop (DDECS)*, pages 15–24, Győr, Hungary, April 2001.
- [202] Erik Jan Marinissen. Philips' Approach to Core-Based System Chip Testing. In *Digest of Papers of IEEE International Workshop on Testing Embedded Core-Based Systems (TECS)*, pages 1.1–1–10, Marina del Rey, CA, USA, May 2001.
- [203] Erik Jan Marinissen. Philips' Approach to Core-Based System Chip Testing. In *Proceedings IFIP International Conference on Very Large Scale Integration (VLSI-SOC)*, pages 201–210, Montpellier, France, December 2001. LIRMM, France.
- [204] Erik Jan Marinissen. An Industrial Approach to Core-Based System Chip Testing. In Michel Robert, Bruno Rouzeyre, Christian Pigué, and Marie-Lise Flottes, editors, *SOC Design Methodologies*, pages 389–400. Kluwer Academic Publishers, 2002.
- [205] Erik Jan Marinissen. The Role of Test Protocols in Automated Test Generation for Embedded-Core-Based System ICs. *Journal of Electronic Testing: Theory and Applications*, 18(4/5):435–454, August 2002.
- [206] Erik Jan Marinissen. The Role of Test Protocols in Automated Test Generation for Embedded-Core-Based System ICs. In Krishnendu Chakrabarty, editor, *SOC (System-on-a-Chip) Testing for Plug and Play Test Automation*, volume 21 of *Frontiers in Electronics Testing*, pages 71–90. Kluwer Academic Publishers, September 2002.
- [207] Erik Jan Marinissen and Joep Aerts. Test Protocol Scheduling for Embedded-Core Based System ICs. In *Digest of Papers of IEEE International Workshop on Testing Embedded Core-Based Systems (TECS)*, pages 5.3–1–9, Washington, DC, USA, October 1998.
- [208] Erik Jan Marinissen et al. A Structured And Scalable Mechanism for Test Access to Embedded Reusable Cores. In *Proceedings IEEE International Test Conference (ITC)*, pages 284–293, Washington, DC, USA, October 1998.
- [209] Erik Jan Marinissen et al. On IEEE P1500's Standard for Embedded Core Test. *Journal of Electronic Testing: Theory and Applications*, 18(4/5):365–383, August 2002.
- [210] Erik Jan Marinissen et al. On IEEE P1500's Standard for Embedded Core Test. In Krishnendu Chakrabarty, editor, *SOC (System-on-a-Chip) Testing for Plug and Play Test Automation*, volume 21 of *Frontiers in Electronics Testing*, pages 1–19. Kluwer Academic Publishers, September 2002.
- [211] Erik Jan Marinissen and Sandeep Kumar Goel. Analysis of Test Bandwidth Utilization in Test Bus and TestRail Architectures for SOCs. In *Proceedings IEEE Design and Diagnostics of Electronic Circuits and Systems Workshop (DDECS)*, pages 52–60, Brno, Czech Republic, April 2002.
- [212] Erik Jan Marinissen and Sandeep Kumar Goel. SOC Test Infrastructure Optimization Under Layout Constraints. In *Proceedings IEEE VLSI Test Symposium (VTS)*, Napa, CA, USA, April 2003.

- [213] Erik Jan Marinissen, Sandeep Kumar Goel, and Maurice Lousberg. Wrapper Design for Embedded Core Test. In *Proceedings IEEE International Test Conference (ITC)*, pages 911–920, Atlantic City, NJ, USA, October 2000.
- [214] Erik Jan Marinissen, Vikram Iyengar, and Krishnendu Chakrabarty. ITC'02 SOC Test Benchmarks Web Site. <http://www.extra.research.philips.com/itc02socbenchm/>.
- [215] Erik Jan Marinissen, Vikram Iyengar, and Krishnendu Chakrabarty. A Set of Benchmarks for Modular Testing of SOCs. In *Proceedings IEEE International Test Conference (ITC)*, pages 519–528, Baltimore, MD, USA, October 2002.
- [216] Erik Jan Marinissen, Rohit Kapur, and Yervant Zorian. On Using IEEE P1500 SECT for Test Plug-n-Play. In *Proceedings IEEE International Test Conference (ITC)*, pages 770–777, Atlantic City, NJ, USA, October 2000.
- [217] Erik Jan Marinissen, Krijn Kuiper, and Clemens Wouters. Test Protocol Expansion in Hierarchical Macro Testing. In *Proceedings IEEE European Test Conference (ETC)*, pages 28–36, Rotterdam, The Netherlands, April 1993.
- [218] Erik Jan Marinissen and Maurice Lousberg. Macro Test: A Liberal Test Approach for Embedded Reusable Cores. In *Digest of Papers of IEEE International Workshop on Testing Embedded Core-Based Systems (TECS)*, pages 1.2–1–9, Washington, DC, USA, November 1997.
- [219] Erik Jan Marinissen and Maurice Lousberg. The Role of Test Protocols in Testing Embedded-Core-Based System ICs. In *Proceedings IEEE European Test Workshop (ETW)*, pages 70–75, Konstanz, Germany, May 1999.
- [220] Erik Jan Marinissen and Tom Waayers. Infrastructure for Modular SOC Testing. In *Proceedings IEEE Custom Integrated Circuits Conference (CICC)*, pages 671–678, Orlando, FL, USA, October 2004.
- [221] Erik Jan Marinissen and Yervant Zorian. Challenges in Testing Core-Based System ICs. *IEEE Communications Magazine*, 37(6):104–109, June 1999.
- [222] Erik Jan Marinissen, Yervant Zorian, Rohit Kapur, Tony Taylor, and Lee Whetsel. Towards a Standard for Embedded Core Test: An Example. In *Proceedings IEEE International Test Conference (ITC)*, pages 616–627, Atlantic City, NJ, USA, September 1999.
- [223] Walid Maroufi, Mounir Benabdenbi, and Meryem Marzouki. Controlling the CAS-BUS TAM With The 1149.1 Features: A Way of Testing Systems on a Chip. In *Digest of Papers of IEEE International Workshop on Testing Embedded Core-Based Systems (TECS)*, pages 4.5–1–6, Montreal, Canada, May 2000.
- [224] F. Martin and C. Papachristou. Microprocessor Based Testing for Core-Based System-on-Chip. In *Digest of Papers of IEEE International Workshop on Testing Embedded Core-Based Systems (TECS)*, pages 2.3–1–6, Dana Point, CA, USA, April 1999.
- [225] Bruce Mathewson. Core Provider's Test Experience. <http://grouper.ieee.org/groups/1500/pastmeetings.html#dac98>, June 1998. Presentation at IEEE P1500 Working Group Meeting, Sunnyvale, CA, USA, June 1998.
- [226] Teresa McLaurin and Rohit Kapur. 'Wrap' Your Cores to Enable SoC Test. *EE Design*, November 24 2004.
- [227] Teresa McLaurin and John C. Potter. On-The-Shelf Core Pattern Methodology for ColdFire Cores. In *Digest of Papers of IEEE International Workshop on Testing Embedded Core-Based Systems (TECS)*, pages 3.1–1–7, Montreal, Canada, May 2000.
- [228] Teresa McLaurin and John C. Potter. On-The-Shelf Core Pattern Methodology for ColdFire Microprocessor Cores. In *Proceedings IEEE International Test Conference (ITC)*, pages 1100–1107, Atlantic City, NJ, USA, October 2000.

- [229] Teresa L. McLaurin, Frank Frederick, and Rich Slobodnik. The Testability Features of the ARM1026EJ Microprocessor Core. In *Proceedings IEEE International Test Conference (ITC)*, pages 773–782, Charlotte, NC, USA, September 2003.
- [230] Micle Moerenhout. Reducing IC Test Time through Parallel Composition of Test Protocols. Master’s thesis, Eindhoven University of Technology, Eindhoven, The Netherlands, January 1996.
- [231] James Monzel and Edward Orosz. Testing ‘Systems-on-a-Chip’ in a Low Cost ASIC Test Environment. In *Digest of Papers of IEEE International Workshop on Testing Embedded Core-Based Systems (TECS)*, pages 5.1–1–8, Washington, DC, USA, November 1997.
- [232] Peter Muhmenthaler and Jürgen Alt. An Approach to Embedded Core-Based Systems Test. In *Digest of Papers of IEEE International Workshop on Testing Embedded Core-Based Systems (TECS)*, pages 1.3–1–3, Washington, DC, USA, November 1997.
- [233] Sobhan Mukherji, Loc Nguyen, Dwayne Burek, and Steve Baird. IP/VC-Based Test Methodology (Part-1): A Case Study. In *Digest of Papers of IEEE International Workshop on Testing Embedded Core-Based Systems (TECS)*, pages 1.2–1–9, Washington, DC, USA, October 1998.
- [234] Fidel Muradali, Rob Aitken, and Neal Jaarsma. System-Level-Integration Test Hardware and its Impact on Reuse and Design. In *Digest of Papers of IEEE International Workshop on Testing Embedded Core-Based Systems (TECS)*, pages 1.1–1–6, Dana Point, CA, USA, April 1999.
- [235] Brian T. Murray. *Hierarchical Testing Using Precomputed Tests for Modules*. PhD thesis, University of Michigan, Ann Arbor, MI, USA, December 1994.
- [236] Brian T. Murray and John P. Hayes. Hierarchical Test Generation Using Precomputed Tests for Modules. *IEEE Transactions on Computer-Aided Design*, 9(6):594–603, June 1990.
- [237] Brian T. Murray and John P. Hayes. Test Propagation Through Modules and Circuits. In *Proceedings IEEE International Test Conference (ITC)*, pages 748–757, Washington, DC, USA, September 1991.
- [238] Brian T. Murray and John P. Hayes. Testing ICs: Getting to the Core of the Problem. *IEEE Computer*, 29(11):32–38, November 1996.
- [239] Mohsen Nahvi and Andre Ivanov. A Packet Switching Communication-Based Test Access Mechanism for System Chips. In *Digest of Papers of IEEE European Test Workshop (ETW)*, pages 195–200, Saltsjobaden, Sweden, May 2001.
- [240] Mohsen Nahvi and Andre Ivanov. An Embedded Autonomous Scan-Based Results Analyzer (EARA) for SoC Cores. In *Proceedings IEEE VLSI Test Symposium (VTS)*, pages 293–298, Napa, CA, USA, April 2003.
- [241] Mohsen Nahvi, Andre Ivanov, and Resve Saleh. Dedicated Autonomous Scan-Based Testing (DAST) for Embedded Cores. In *Proceedings IEEE International Test Conference (ITC)*, pages 1176–1183, Baltimore, MD, USA, October 2002.
- [242] D. Nikolos, Th. Haniotakis, H.T. Vergos, and Y. Tsiatouhas. Path Delay Fault Testing of ICs with Embedded Intellectual Property Blocks. In *Proceedings Design, Automation, and Test in Europe (DATE)*, pages 112–116, Munich, Germany, March 1999.
- [243] Mehrdad Nourani and Chris Papachristou. Parallelism in Structural Fault Testing of Embedded Cores. In *Proceedings IEEE VLSI Test Symposium (VTS)*, pages 15–20, Monterey, CA, USA, April 1998.
- [244] Mehrdad Nourani and Chris Papachristou. Structural Fault Testing of Embedded Cores Using Pipelining. *Journal of Electronic Testing: Theory and Applications*, 15(1):129, 1999.

- [245] Mehrdad Nourani and Chris Papachristou. An ILP Formulation to Optimize Test Access Mechanism in System-on-Chip Testing. In *Proceedings IEEE International Test Conference (ITC)*, pages 902–910, Atlantic City, NJ, USA, October 2000.
- [246] Ishwar Parulkar et al. A Scalable, Low Cost Design-for-Test Architecture for UltraSPARC Chip Multi-Processors. In *Proceedings IEEE International Test Conference (ITC)*, pages 726–735, Baltimore, MD, USA, October 2002.
- [247] Ilia Polian and Bernd Becker. Reducing ATE Cost in System-on-Chip Test. In *Digest of Papers of IEEE International Workshop on Test Resource Partitioning (TRP)*, pages 1–8, Napa, CA, USA, April 2003.
- [248] Irith Pomeranz and Yervant Zorian. On Providing a Set of Alternative Tests for an Embedded Core by Test-Point Insertion. In *Digest of Papers of IEEE International Workshop on Testing Embedded Core-Based Systems (TECS)*, pages 2.3–1–8, Washington, DC, USA, November 1997.
- [249] Irith Pomeranz and Yervant Zorian. Issues in Testing of Non-Isolated Embedded Cores and their Surrounding Logic. In *Digest of Papers of IEEE International Workshop on Testing Embedded Core-Based Systems (TECS)*, pages 2.1–1–7, Washington, DC, USA, October 1998.
- [250] Irith Pomeranz and Yervant Zorian. On Testing of Non-Isolated Embedded Legacy Cores and their Surrounding Logic. In *Proceedings IEEE VLSI Test Symposium (VTS)*, pages 41–48, Dana Point, CA, USA, April 1999.
- [251] Irith Pomeranz and Yervant Zorian. On Testing of Non-Isolated Sequential Embedded Legacy Cores and their Surrounding Logic. In *Digest of Papers of IEEE International Workshop on Testing Embedded Core-Based Systems (TECS)*, pages 2.2–1–7, Dana Point, CA, USA, April 1999.
- [252] Irith Pomeranz and Yervant Zorian. On Design-for-Testability for Circuits Comprised of Non-Isolated Legacy Cores. In *Digest of Papers of IEEE International Workshop on Testing Embedded Core-Based Systems (TECS)*, pages 2.1–1–7, Montreal, Canada, May 2000.
- [253] Irith Pomeranz and Yervant Zorian. Using a Scan Simulation Model of a Random-Logic Embedded Core to Facilitate Test Generation for the Surrounding Logic. In *Digest of Papers of IEEE International Workshop on Testing Embedded Core-Based Systems (TECS)*, pages 2.3–1–7, Marina del Rey, CA, USA, May 2001.
- [254] Julien Pouget, Erik Larsson, Zebo Peng, Marie-Lise Flottes, and Bruno Rouzeyre. An Efficient Approach to SoC Wrapper Design, TAM Configuration and Test Scheduling. In *Proceedings IEEE European Test Workshop (ETW)*, pages 51–56, Maastricht, The Netherlands, May 2003.
- [255] Bahram Pouya and Nur Touba. Modifying User-Defined Logic for Test Access to Embedded Cores. In *Proceedings IEEE International Test Conference (ITC)*, pages 60–68, Washington, DC, USA, November 1997.
- [256] Marinés Puig-Medina, Gulbin Ezer, and Pavlos Konas. Verification of Configurable Processor Cores. In *Proceedings ACM/IEEE Design Automation Conference (DAC)*, pages 426–431, Los Angeles, CA, USA, June 2000. Association for Computing Machinery, Inc.
- [257] Md. Saffat Quasem and Sandeep K. Gupta. Test Information for Cores: Comparative Analysis and Recommendations. In *Digest of Papers of IEEE International Workshop on Testing Embedded Core-Based Systems (TECS)*, pages 2.3–1–4, Montreal, Canada, May 2000.
- [258] Janusz Rajski, Tom Eberle, and Jerzy Tyszer. Modular Logic Built-In Self-Test for IP Cores. In *Digest of Papers of IEEE International Workshop on Testing Embedded Core-Based Systems (TECS)*, pages 3.3–1–5, Washington, DC, USA, November 1997.
- [259] Janusz Rajski and Jerzy Tyszer. Modular Logic Built-In Self Test for IP Cores. In *Proceedings IEEE International Test Conference (ITC)*, pages 313–321, Washington, DC, USA, October 1998.

- [260] Rochit Rajsuman. Challenge of the 90's: Testing CoreWareTM Based ASICs. In *Proceedings IEEE International Test Conference (ITC)*, Washington, DC, USA, November 1996.
- [261] Rochit Rajsuman. A New Test Methodology for Testing Embedded Memories in Core Based System-on-a-Chip ICs. In *Digest of Papers of IEEE International Workshop on Testing Embedded Core-Based Systems (TECS)*, pages 3.4–1–6, Washington, DC, USA, October 1998.
- [262] Rochit Rajsuman. Testing a System-on-a-Chip with Embedded Microprocessor. In *Proceedings IEEE International Test Conference (ITC)*, pages 499–508, Atlantic City, NJ, USA, September 1999.
- [263] S. Ravi, N. Jha, and G. Lakshiminarayana. A Framework for Testing Core-Based Systems-on-a-Chip. In *Proceedings International Conference on Computer-Aided Design (ICCAD)*, San Jose, CA, USA, November 1999.
- [264] Jeff Remmers, Moe Villalba, and Richard Fisette. Hierarchical DFT Methodology – A Case Study. In *Proceedings IEEE International Test Conference (ITC)*, pages 847–856, Charlotte, NC, USA, October 2004.
- [265] Detlev Richter and Volker Kilian. The Embedded DRAM Test Dilemma. In *Digest of Papers of IEEE International Workshop on Testing Embedded Core-Based Systems (TECS)*, pages 3.3–1–6, Dana Point, CA, USA, April 1999.
- [266] Ann Marie Rincon et al. Core Design and System-on-a-Chip Integration. *IEEE Design & Test of Computers*, 14(4):26–35, December 1997.
- [267] Paul Rosinger, Bashir Al-Hashimi, and Nicola Nicolici. Power Constrained Test Scheduling Using Power Profile Manipulation. In *Proceedings International Symposium on Circuits and Systems (ISCAS)*, volume V, pages V251–V254, May 2001.
- [268] Don E. Ross, Tim Wood, and Grady Giles. Conversion of Small Functional Test Sets of Nonscan Blocks to Scan Patterns. In *Proceedings IEEE International Test Conference (ITC)*, pages 691–700, Atlantic City, NJ, USA, October 2000.
- [269] Zahra sadat Ebadi and Andre Ivanov. Design of an Optimal Test Access Architecture Using a Genetic Algorithm. In *Proceedings IEEE Asian Test Symposium (ATS)*, pages 205–210, Kyoto, Japan, November 2001.
- [270] Zahra sadat Ebadi and Andre Ivanov. Time Domain Multiplexed TAM: Implementation and Comparison. In *Proceedings Design, Automation, and Test in Europe (DATE)*, pages 732–737, Munich, Germany, March 2003.
- [271] Jayashree Saxena, Paul Policke, Ken Cyr, Agapito Benavides, and Harry Malpass. Test Strategy for TI's TMS320AV7100 Device. In *Digest of Papers of IEEE International Workshop on Testing Embedded Core-Based Systems (TECS)*, pages 3.2–1–6, Washington, DC, USA, October 1998.
- [272] Anuja Sehgal and Krishnendu Chakrabarty. Efficient Modular Testing of SOCs Using Dual-Speed TAM Architectures. In *Proceedings Design, Automation, and Test in Europe (DATE)*, pages 422–427, Paris, France, February 2004.
- [273] Anuja Sehgal, Jeff Fitzgerald, and Jeff Rearick. Test Cost Reduction for the AMDTM Athlon Processor using Test Partitioning. In *Proceedings IEEE International Test Conference (ITC)*, Santa Clara, CA, USA, October 2007.
- [274] Anuja Sehgal, Sandeep Kumar Goel, Erik Jan Marinissen, and Krishnendu Chakrabarty. IEEE P1500-Compliant Test Wrapper Design for Hierarchical Cores. In *Proceedings IEEE International Test Conference (ITC)*, pages 1203–1212, Charlotte, NC, USA, October 2004.
- [275] Anuja Sehgal, Sandeep Kumar Goel, Erik Jan Marinissen, and Krishnendu Chakrabarty. Hierarchy-Aware and Area-Efficient Test Infrastructure Design for Core-Based System Chips. In *Proceedings Design, Automation, and Test in Europe (DATE)*, pages 285–290, Munich, Germany, March 2006.

- [276] Anuja Sehgal, Vikram Iyengar, Mark D. Krasniewski, and Krishnendu Chakrabarty. Test Cost Reduction for SOCs Using Virtual TAMs and Lagrange Multipliers. In *Proceedings ACM/IEEE Design Automation Conference (DAC)*, pages 738–743, Anaheim, CA, USA, June 2003.
- [277] Geert Seuren and Tom Waayers. Extending the Digital Core-Based Test Methodology to Support Mixed-Signal. In *Proceedings IEEE International Test Conference (ITC)*, pages 281–289, Charlotte, NC, USA, October 2004.
- [278] Markus Seuring and Krishnendu Chakrabarty. Space Compaction of Test Responses for IP Cores using Orthogonal Transmission Functions. In *Proceedings IEEE VLSI Test Symposium (VTS)*, pages 213–219, Montreal, Canada, April 2000.
- [279] Ozgur Sinanoglu and Erik Jan Marinissen. Analysis of the Test Data Volume Reduction Benefit of Modular SOC Testing. In *Proceedings Design, Automation, and Test in Europe (DATE)*, pages 182–187, Munich, Germany, March 2008.
- [280] Ozgur Sinanoglu and Alex Orailoglu. Autonomous Yet Deterministic Test of SOC Cores. In *Proceedings IEEE International Test Conference (ITC)*, pages 1359–1368, Charlotte, NC, USA, October 2004.
- [281] Gary Smith. Test and System Level Integration. *IEEE Design & Test of Computers*, 14(4):19, December 1997.
- [282] Jaehoon Song and Sungju Park. A Simple Wrapped Core Linking Module for SoC Test Access. In *Proceedings IEEE Asian Test Symposium (ATS)*, pages 344–349, Tamuning, Guam, USA, November 2002.
- [283] Maurizio Spadari, Ted Vaida, and Pradipta Ghosh. A Hierarchical Test Methodology Involving Multiple Embedded Cores Having Different DfT Mechanisms. In *Digest of Papers of IEEE International Workshop on Testing Embedded Core-Based Systems (TECS)*, pages 1.4–1–8, Dana Point, CA, USA, April 1999.
- [284] B.S. Srinivasa, M.S. Rao, J. Abraham, and R.A. Parekhji. Design for Test in TMS320C27xx: Techniques for Achieving High Fault Coverage in Embedded Cores. In *Digest of Papers of IEEE International Workshop on Testing Embedded Core-Based Systems (TECS)*, pages 3.2–1–11, Dana Point, CA, USA, April 1999.
- [285] Milan Stancic et al. A New Test Generation Approach for Embedded Analogue Cores in SoC. In *Proceedings IEEE International Test Conference (ITC)*, pages 861–869, Baltimore, MD, USA, October 2002.
- [286] Chauchin Su and Wenliang Tseng. Configuration Free SoC Interconnect BIST Methodology. In *Proceedings IEEE International Test Conference (ITC)*, pages 1033–1038, Baltimore, MD, USA, October 2001.
- [287] Chih-Ping Su and Cheng-Wen Wu. Graph-Based Power-Constrained Test Scheduling for SOC. In *Proceedings IEEE Design and Diagnostics of Electronic Circuits and Systems Workshop (DDECS)*, pages 61–68, Brno, Czech Republic, April 2002.
- [288] Makoto Sugihara, Hiroshi Date, and Hiroto Yasuura. A Novel Test Methodology for Core-Based System LSIs and a Testing Time Minimization Problem. In *Proceedings IEEE International Test Conference (ITC)*, pages 465–472, Washington, DC, USA, October 1998.
- [289] Tony Taylor et al. A Test Language for Core Based Test. In *Digest of Papers of IEEE International Workshop on Testing Embedded Core-Based Systems (TECS)*, pages 3.1–1–8, Marina del Rey, CA, USA, May 2001.
- [290] Nur Touba and Bahram Pouya. Testing Embedded Cores Using Partial Isolation Rings. In *Proceedings IEEE VLSI Test Symposium (VTS)*, pages 10–16, Monterey, CA, USA, April 1997.

- [291] Nur Touba and Bahram Pouya. Using Partial Isolation Rings to Test Core-Based Designs. *IEEE Design & Test of Computers*, 14(4):52–59, December 1997.
- [292] S. Tragoudas and M. Michael. A Method for Path Delay Fault ATPG in Embedded Cores. In *Digest of Papers of IEEE International Workshop on Testing Embedded Core-Based Systems (TECS)*, pages 2.1–1–8, Dana Point, CA, USA, April 1999.
- [293] Jos van Beers and Harry van Herten. Test Features of a Core-Based Co-Processor Array for Video Applications. In *Proceedings IEEE International Test Conference (ITC)*, pages 638–647, Atlantic City, NJ, USA, September 1999.
- [294] Michael van Wijngaarden. Test Protocol Expansion: Models and Solution Approaches. Master's thesis, Eindhoven University of Technology, Eindhoven, The Netherlands, August 1993.
- [295] Prab Varma. Evolving Strategies for Testing Systems on Silicon. *Integrated System Design- Virtual Chip Design Supplement*, September 1997.
- [296] Prab Varma and Sandeep Bhatia. A Structured Test Re-Use Methodology for Systems on Silicon. In *Digest of Papers of IEEE International Workshop on Testing Embedded Core-Based Systems (TECS)*, pages 3.1–1–8, Washington, DC, USA, November 1997.
- [297] Prab Varma and Sandeep Bhatia. A Structured Test Re-Use Methodology for Core-Based System Chips. In *Proceedings IEEE International Test Conference (ITC)*, pages 294–302, Washington, DC, USA, October 1998.
- [298] H.J. Vermaak and H.G. Kerckhoff. Enhanced P1500 Compliant Wrapper suitable for Delay Fault Testing of Embedded Cores. In *Digest of Papers of IEEE European Test Workshop (ETW)*, pages 257–262, Maastricht, The Netherlands, May 2003.
- [299] Bart Vermeulen, Steven Oostdijk, and Frank Bouwman. Test and Debug Strategy of a Nexperia™ Digital Video Platform System Chips. In *Digest of Papers of IEEE European Test Workshop (ETW)*, pages 129–138, Saltsjobaden, Sweden, May 2001.
- [300] Bart Vermeulen, Steven Oostdijk, and Frank Bouwman. Test and Debug Strategy of the PNX8525 Nexperia™ Digital Video Platform System Chip. In *Proceedings IEEE International Test Conference (ITC)*, pages 121–130, Baltimore, MD, USA, October 2001.
- [301] Bart Vermeulen, Tom Waayers, and Sjaak Bakker. IEEE 1149.1-Compliant Access Architecture for Multiple Core Debug on Digital System Chips. In *Proceedings IEEE International Test Conference (ITC)*, pages 55–63, Baltimore, MD, USA, October 2002.
- [302] Bart Vermeulen, Tom Waayers, and Sandeep Kumar Goel. Core-Based Scan Architecture for Silicon Debug. In *Proceedings IEEE International Test Conference (ITC)*, pages 638–647, Baltimore, MD, USA, October 2002.
- [303] Ramakrishna Voorakaranam and Abhijit Chatterjee. Hierarchical Test Generation for Analog Circuits Using Incremental Test Development. In *Proceedings IEEE VLSI Test Symposium (VTS)*, pages 296–301, Dana Point, CA, USA, April 1999.
- [304] VSIA. Virtual Socket Interface Alliance Web Site. <http://www.vsi.org/>.
- [305] Tom Waayers. An Improved Test Control Architecture and Test Control Expansion for Core-Based System Chips. In *Proceedings IEEE International Test Conference (ITC)*, pages 1145–1154, Charlotte, NC, USA, September 2003.
- [306] Tom Waayers. An Improved Test Control Architecture for Core-Based System Chips. In *Digest of Papers of IEEE European Test Workshop (ETW)*, pages 333–338, Maastricht, The Netherlands, May 2003.

- [307] Tom Waayers, Erik Jan Marinissen, and Maurice Lousberg. IEEE Std 1500 Compliant Infrastructure for Modular SOC Testing. In *Proceedings IEEE Asian Test Symposium (ATS)*, page 450, Kolkata, India, December 2005.
- [308] Tom Waayers, Richard Morren, and Roberto Grandi. Definition of a Robust Modular SOC Test Architecture; Resurrection of the Single TAM Daisy-Chain. In *Proceedings IEEE International Test Conference (ITC)*, Austin, TX, USA, November 2005.
- [309] Michael G. Wahl et al. The P1500 DFT Disclosure Document: A Standard to Communicate Mergeable Core DFT Data. In *Proceedings IEEE International Test Conference (ITC)*, pages 998–1007, Charlotte, NC, USA, September 2003.
- [310] Chih-Wea Wang et al. Test Scheduling of BISTed Memory Cores for SOC. In *Proceedings IEEE Asian Test Symposium (ATS)*, pages 356–361, Tamuning, Guam, USA, November 2002.
- [311] Lee Whetsel. An IEEE 1149.1 Based Test Access Architecture for ICs with Embedded Cores. In *Proceedings IEEE International Test Conference (ITC)*, pages 69–78, Washington, DC, USA, November 1997.
- [312] Lee Whetsel. Addressable Test Ports - An Approach to Testing Embedded Cores. In *Digest of Papers of IEEE International Workshop on Testing Embedded Core-Based Systems (TECS)*, pages 1.1–1–8, Washington, DC, USA, October 1998.
- [313] Lee Whetsel. Core Test Connectivity, Communication, & Control. In *Proceedings IEEE International Test Conference (ITC)*, pages 303–312, Washington, DC, USA, October 1998.
- [314] Lee Whetsel. Addressable Test Ports: An Approach to Testing Embedded Cores. In *Proceedings IEEE International Test Conference (ITC)*, pages 1055–1064, Atlantic City, NJ, USA, September 1999.
- [315] Lee Whetsel and Mike Ricchetti. Tapping into IEEE P1500 Domains. In *Digest of Papers of IEEE International Workshop on Testing Embedded Core-Based Systems (TECS)*, pages 3.2–1–7, Marina del Rey, CA, USA, May 2001.
- [316] Qiang Xu and Nicola Nicolici. Delay Fault Testing of Core-Based Systems-on-a-Chip. In *Proceedings Design, Automation, and Test in Europe (DATE)*, pages 744–749, Munich, Germany, March 2003.
- [317] Qiang Xu and Nicola Nicolici. On Reducing Wrapper Boundary Register Cells in Modular SOC Testing. In *Proceedings IEEE International Test Conference (ITC)*, pages 622–631, Charlotte, NC, USA, September 2003.
- [318] Qiang Xu and Nicola Nicolici. Time/Area Tradeoffs in Testing Hierarchical SOCs with Hard Mega-Cores. In *Proceedings IEEE International Test Conference (ITC)*, pages 1196–1202, Charlotte, NC, USA, October 2004.
- [319] Qiang Xu and Nicola Nicolici. Wrapper Design for Testing IP Cores with Multiple Clock Domains. In *Proceedings Design, Automation, and Test in Europe (DATE)*, pages 416–421, Paris, France, February 2004.
- [320] Qiang Xu and Nicola Nicolici. Resource-Constrained System-on-a-Chip Test: A Survey. *IEE Proceedings, Computers and Digital Techniques*, 152(4/5):67–81, January 2005.
- [321] Tomokazu Yoneda and Hideo Fujiwara. A DfT Method for Core-Based Systems-on-a-Chip based on Consecutive Testability. In *Proceedings IEEE Asian Test Symposium (ATS)*, pages 193–198, Kyoto, Japan, November 2001.
- [322] Tomokazu Yoneda and Hideo Fujiwara. Design for Consecutive Testability of System-on-a-Chip with Built-In Self Testable Cores. *Journal of Electronic Testing: Theory and Applications*, 18(4/5):487–501, August 2002.

- [323] Tomokazu Yoneda and Hideo Fujiwara. Design for Consecutive Testability of System-on-a-Chip with Built-In Self Testable Cores. In Krishnendu Chakrabarty, editor, *SOC (System-on-a-Chip) Testing for Plug and Play Test Automation*, volume 21 of *Frontiers in Electronics Testing*, pages 123–137. Kluwer Academic Publishers, September 2002.
- [324] Tomokazu Yoneda and Hideo Fujiwara. Design for Consecutive Transparency of Cores in System-on-a-Chip. In *Proceedings IEEE VLSI Test Symposium (VTS)*, pages 287–292, Napa, CA, USA, April 2003.
- [325] Tomokazu Yoneda, Masahiro Imanishi, and Hideo Fujiwara. An SOC Test Scheduling Algorithm using Reconfigurable Union Wrappers. In *Proceedings Design, Automation, and Test in Europe (DATE)*, pages 231–236, Nice, France, April 2007.
- [326] Tomokazu Yoneda, Tetsuo Uchiyama, and Hideo Fujiwara. Area and Time Co-Optimization for System-on-a-Chip based on Consecutive Testability. In *Proceedings IEEE International Test Conference (ITC)*, pages 415–422, Charlotte, NC, September 2003.
- [327] Daniella Zhao and S. Upadhyaya. Dynamically Partitioned Test Scheduling with Adaptive TAM Configuration for Power-Constrained SoC Testing. *IEEE Transactions on Computer-Aided Design*, 24(6):956–965, June 2005.
- [328] Vladimir Zivkovic, Ronald Tangelder, and Hans Kerkhoff. Test-Pattern Generation and Fault Coverage Determination of Embedded Cores. In *Proceedings IEEE European Test Workshop (ETW)*, Konstanz, Germany, May 1999.
- [329] Vladimir Zivkovic, Ronald Tangelder, and Hans Kerkhoff. Computer-Aided Test Flow in Core Based Design. In *International Conference on Microelectronics*, pages 715–718, Nis, Yugoslavia, May 2000.
- [330] Vladimir Zivkovic, Ronald Tangelder, and Hans Kerkhoff. Computer-Aided Test Flow in Core Based Design. *Elsevier Journal of Microelectronics*, 31(11/12):999–1008, November 2000.
- [331] Yervant Zorian. A Distributed BIST Control Scheme for Complex VLSI Devices. In *Proceedings IEEE VLSI Test Symposium (VTS)*, pages 6–11, Princeton, NJ, USA, April 1993.
- [332] Yervant Zorian. Test Requirements for Embedded Core-Based Systems and IEEE P1500. In *Proceedings IEEE International Test Conference (ITC)*, pages 191–199, Washington, DC, USA, November 1997.
- [333] Yervant Zorian, Dwayne Burek, and R. Chandramouli. A 2-Step Strategy tackles System-on-a-Chip Test. In *Digest of Papers of IEEE International Workshop on Testing Embedded Core-Based Systems (TECS)*, pages 3.2–1–5, Washington, DC, USA, November 1997.
- [334] Yervant Zorian et al. IP and Automation to Support IEEE P1500. In *Proceedings IEEE VLSI Test Symposium (VTS)*, page 411, Marina del Rey, CA, USA, May 2000.
- [335] Yervant Zorian and Erik Jan Marinissen. System Chip Test: How Will It Impact Your Design? In *Proceedings ACM/IEEE Design Automation Conference (DAC)*, pages 136–141, Los Angeles, CA, USA, June 2000. Association for Computing Machinery, Inc.
- [336] Yervant Zorian, Erik Jan Marinissen, and Sujit Dey. Testing Embedded-Core Based System Chips. In *Proceedings IEEE International Test Conference (ITC)*, pages 130–143, Washington, DC, USA, October 1998.
- [337] Yervant Zorian, Erik Jan Marinissen, and Sujit Dey. Testing Embedded-Core-Based System Chips. *IEEE Computer*, 32(6):52–60, June 1999.
- [338] Wei Zou, Sudhakar M. Reddy, Irith Pomeranz, and Yu Huang. SOC Test Scheduling Using Simulated Annealing. In *Proceedings IEEE VLSI Test Symposium (VTS)*, pages 325–330, Napa, CA, USA, April 2003.