A Set of Benchmarks for Modular Testing of SOCs

Erik Jan Marinissen *
Philips Research Laboratories
Eindhoven, The Netherlands

Vikram Iyengar
IBM Microelectronics
Essex Jct, VT, USA

Krish Chakrabarty
Duke University
Durham, NC, USA

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1. Introduction

- System Chips or SOCs
  - 'Complete system' integrated onto single die
  - Enabled by semiconductor process and design technology
  - Test development is challenging
    - Heterogeneous mix of circuit structures and design styles
    - Very large size
- Modular test approach for large SOCs
  - Non-logic blocks
  - IP cores
  - Divide-n-Conquer
  - Test Re-Use
- Research challenges include
  - Automated design of test access infrastructure
  - Automated test scheduling

1. Introduction

Benchmark Initiative

Goals

- Stimulate research into modular SOC testing
- Make realistic SOC data available to (academic) researchers
- Enable objective comparison of research results

Disclaimer

- Use of benchmarks is limited in scope to modular testing of SOCs
- Benchmarks *cannot* be used for problems that require
  - Internal details of SOC implementation (e.g., fault modeling, fault diagnosis, test generation)
  - Detailed values of the test pattern sets (e.g., test data compression)

A Set of Benchmarks for Modular Testing of SOCs

Outline of This Presentation

1. Introduction
2. Prior Work in Benchmarks
3. Benchmark Format
4. Benchmark Naming
5. Benchmark Set
6. Classification of Problems and Prior Work
7. Conclusion

2. Prior Work in Benchmarks
ISCAS'85 / ISCAS'89 Benchmarks

- ISCAS'85 Benchmarks [Brglez & Fujiwara – ISCAS'85]
  - 10 combinational circuits: c432, c499, …, c7552
- ISCAS'89 Benchmarks [Brglez, Bryan, Kozminski – ISCAS'89]
  - 31 sequential circuits: s27, s208.1, …, s38584.1

- Positive
  - Homogeneous set
  - Neutral netlist language
  - Meaningful benchmark names
  - Freely available to anyone
  - Downloadable through Internet
- Negative
  Not representative of today's industrial SOCs
  - Too small in size
  - Gate-level only, no RTL
  - Logic only, no embedded memories nor analog
  - No multiple clock domains
  - No bidirs and tri-states

2. Prior Work in Benchmarks
ITC'99 Benchmarks

- ITC'99 Benchmarks [Davidson – ITC'99]
  - Attempt to overcome the drawbacks of the ISCAS benchmarks
  - 32 circuits:
    I991, I992, I993, I994, I995, I99T<b1-b22>, I99S<1-4>, I99C1

- Positive
  - More representative of today's industrial SOCs
  - Downloadable through Internet
- Negative
  Heterogeneous set
  - Academic vs. industrial
  - Combinational vs. sequential
  - Gate-level vs. RT-level
  - With vs. without memories
  - Freely available vs. Community Source License

2. Prior Work in Benchmarks

Goals for ITC'02 SOC Test Benchmarks

- Combine strengths of prior benchmarking activities
  - ISCAS'85/'89: • Homogeneous set of SOCs, to allow experimental on sets of SOCs
    • Meaningful benchmark names
    • Freely available to anyone
  - ITC'99 : • Representative of today's industrial SOCs
  - Common : • Downloadable through Internet
- Restrict IP released through benchmark data
  - Allow companies to contribute real-life SOC data
- Benchmark data should still allow useful research

3. Benchmark Format

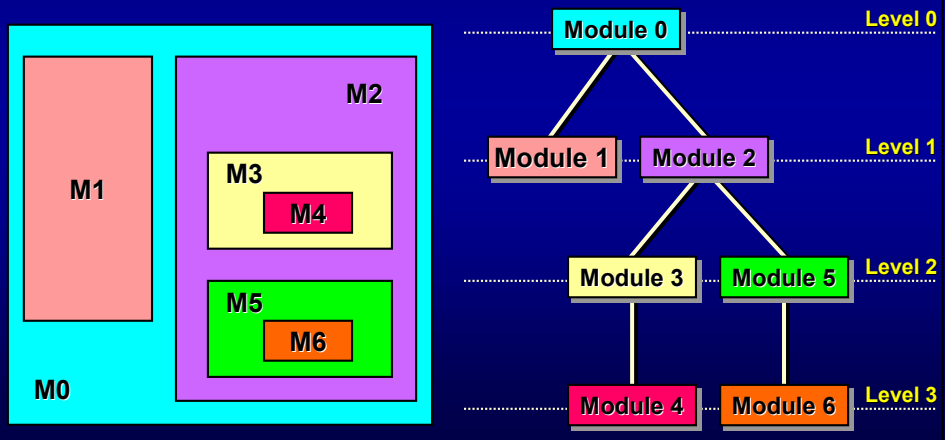
SOC Test Information

- SOC name
- # Modules
- Global option settings: layout, power
- Per module
  - Level in design hierarchy
  - # Inputs, # outputs, # bidirs
  - # Scan chains, scan chain lengths
  - Layout position of module (optional)
  - # Tests
  - Per test
    - Usage of scan chains
    - Number of test patterns
    - Power dissipation (optional)

3. Benchmark Format

SOC Design Hierarchy

- All stand-alone testable units are *'modules'*
- SOC is 'Module 0' by definition



3. Benchmark Format

Example SOC Benchmark

```
SocName x847
TotalModules 7
Options Power 1 XY 1

Module 0 Level 0 Inputs 312 Outputs 312 Bidirs 0 ScanChains 2 : 54 43
Module 0 X -1 Y -1
Module 0 TotalTests 2
Module 0 Test 1 ScanUse 1 TamUse 0 Patterns 43 Power 128
Module 0 Test 2 ScanUse 0 TamUse 0 Patterns 32 Power 537

Module 1 Level 1 Inputs 10 Outputs 11 Bidirs 12 ScanChains 4 : 20 21 22 23
Module 1 X 678 Y 123
Module 1 TotalTests 3
Module 1 Test 1 ScanUse 1 TamUse 1 Patterns 567 Power 576
Module 1 Test 2 ScanUse 1 TamUse 1 Patterns 876 Power 275
Module 1 Test 3 ScanUse 0 TamUse 1 Patterns 908 Power 123
…
```

4. Benchmark Naming

Naming Inspiration

ISCAS'85 / ISCAS'89 benchmarks [Brglez et al. – ISCAS'85/'89]
c432 – c7552, s27 – s38584.1

- First letter indicates 'combinational' vs. 'sequential'
- Number represents number of nets, representative measure of benchmark complexity

Philips benchmarks [Kiefer et al. – ITC'00]
p2441 – p80590

- First letter refers to benchmark contributor
- Number represents number of nets, representative measure of benchmark complexity

4. Benchmark Naming

Benchmark Naming Scheme

- One letter, followed by a number
- Letter refers to contributor of benchmark SOC
  - 'c' and 's' are not used, in order to avoid confusing with ISCAS'85 / '89
  - 'x' is reserved for anonymous benchmark contributors
  - Other letters are given out on 'first-come-first-serve' basis
- Number according to formula [Iyengar et al. – ITC'01]

$$\left\lceil \frac{|T| \cdot \sum_{t \in T} tu_t \cdot p_t \cdot \left(i_{m(t)} + o_{m(t)} + b_{m(t)} + su_t \cdot \sum_{x=1}^{Sm(t)} l_{m(t),\,x} \right)}{10{,}000} \right\rceil$$

5. Benchmark Set

Status

Benchmarks

- Freely downloadable through Internet
- Currently 12 SOC benchmarks
  - 5 from academic contributors
  - 7 from industrial contributors

  More contributions pending

Awareness, Interest, Usage

- E-mail reflector with 43 subscribers
- Awareness panel session at TECS'02:
  'How Useful Are The ITC'02 SOC Test Benchmarks?'
  - Panel report in 'IEEE Design & Test of Computers' – 10/2002
- Special session at ITC'02 + papers in other sessions
- Research papers using the benchmarks:
  DDECS'02, VTS'02, ETW'02, NATW'02, DAC'02, ITC'02, ATS'02, DATE'03, JETTA, TCAD, TComp, …

5. Benchmark Set

Benchmark Set + Contributors

u226	Univ. Fed. Rio Grande do Sul
d281, d695	Duke University
h953	National Tsing Hua University
g1023	Universität Stuttgart

academic

industrial

f2126	Faraday Technologies
q12710	Hewlett-Packard
p22810, p34392, p93791	Philips Electronics
t512505	Texas Instruments
a586710	Analog Devices

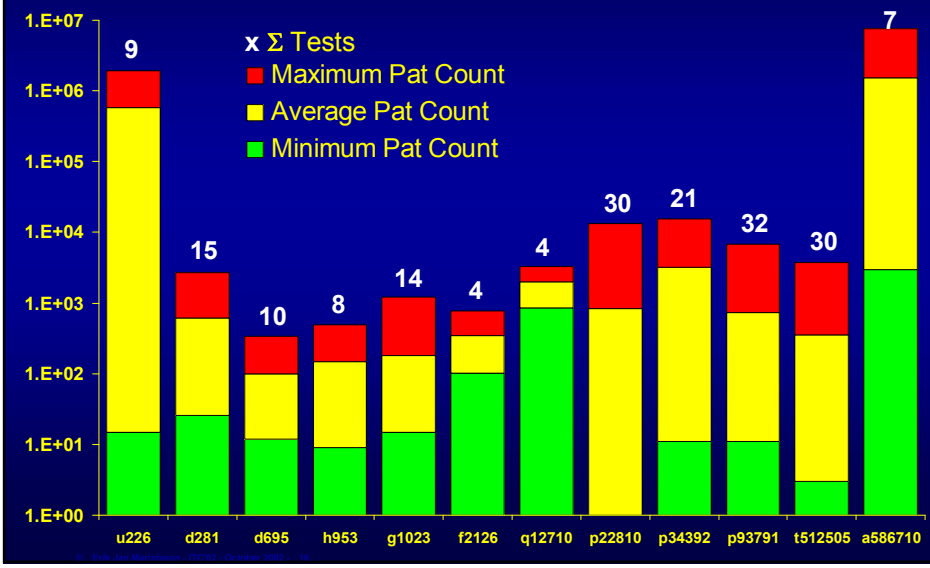
5. Benchmark Set

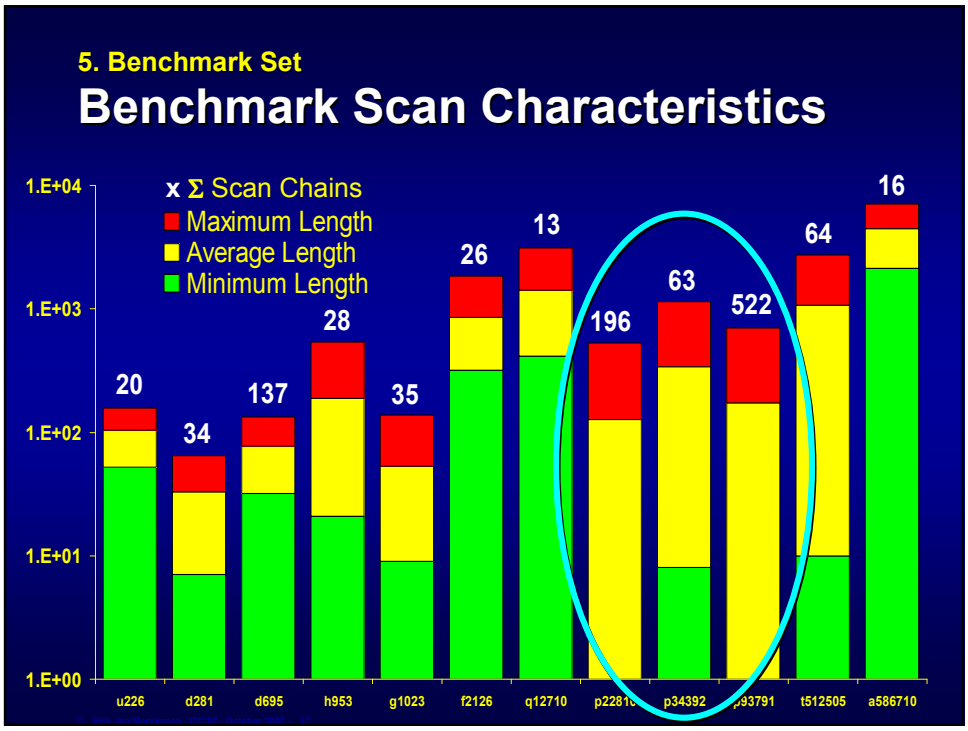
Benchmarks Characteristics

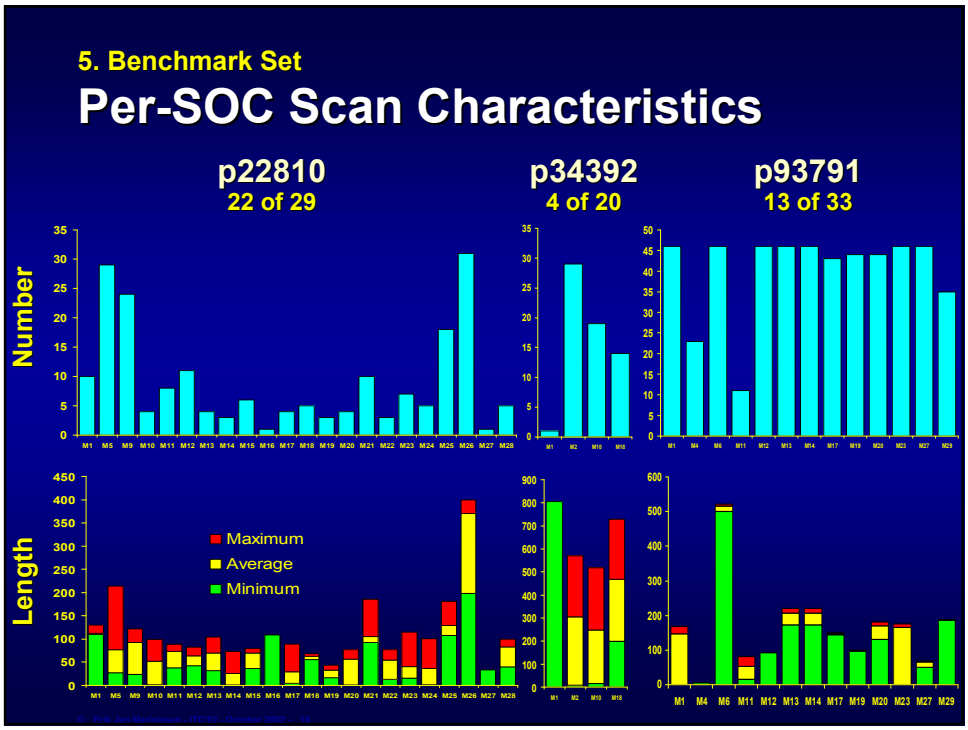
SOC	# Modules	# Levels	# Tests	Σ # I/Os	Σ # SFFs	Σ # Pats
u226	10	2	9	376	1040	5148569
d281	9	2	15	2931	882	8818
d695	11	2	10	1845	6384	881
h953	9	2	8	929	4657	1100
g1023	15	2	14	3707	1546	2349
f2126	5	2	4	1597	13996	962
q12710	5	2	4	13167	12991	4612
p22810	29	3	30	4283	24723	24890
p34392	20	3	21	2057	20948	66349
p93791	33	3	32	6943	89973	22987
t512505	31	2	30	8663	68051	10479
a568710	8	3	7	3755	37656	10850894

5. Benchmark Set

Benchmark Test Set Characteristics



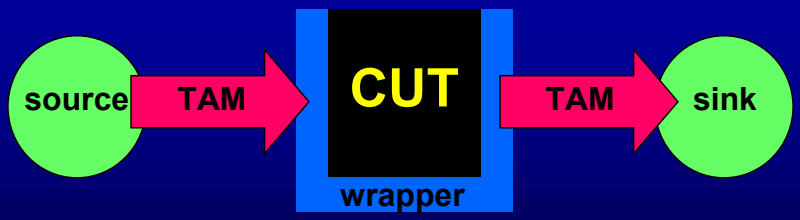

5. Benchmark Set
Benchmark Scan Characteristics
x Σ Scan Chains
Maximum Length
Average Length
Minimum Length
1.E+04
1.E+03
1.E+02
1.E+01
1.E+00
20
34
137
28
35
26
13
196
63
522
64
16
u226
d281
d695
h953
g1023
f2126
q12710
p22810
p34392
p93791
t512505
a586710


5. Benchmark Set
Per-SOC Scan Characteristics
p22810
22 of 29
p34392
4 of 20
p93791
13 of 33
Number
Length
Maximum
Average
Minimum

6. Classification of Problems and Prior Work

Are These Benchmarks Useful?

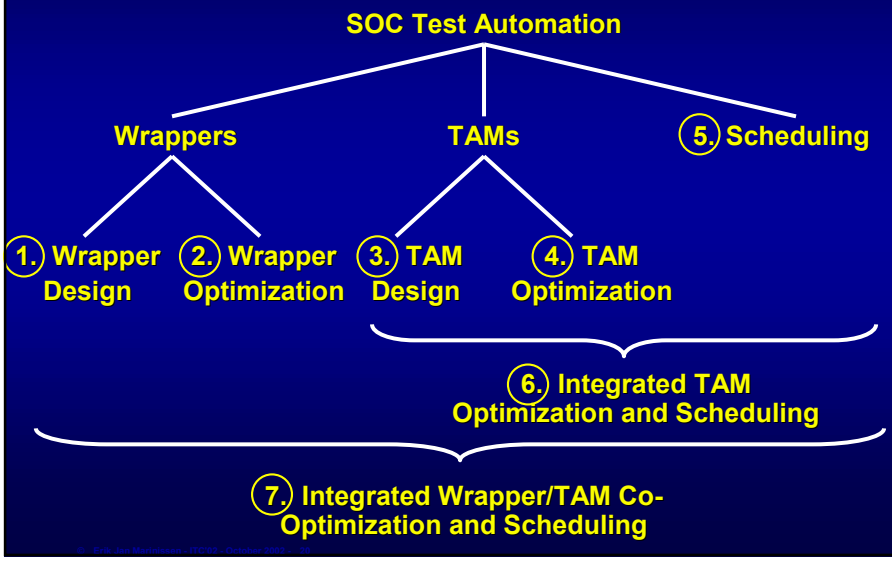
- Benchmark data lacks details on
  - Module implementation
  - Test pattern contents
- For what research problems can these benchmarks be used?



[Zorian, Marinissen, Dey - ITC'98]

6. Classification of Problems and Prior Work

Classification of Problems



6. Classification of Problems and Prior Work

Wrapper Design + Optimization

1. Wrapper Design
- Partial isolation rings [Touba & Pouya – D&T'97]
- Test collar [Varma & Bhatia – ITC'98]
- TestShell [Marinissen et al. – ITC'98]
- IEEE P1500 SECT [Marinissen et al. – JETTA'02]

2. Wrapper Optimization
- Efficient de-serialization through balanced wrapper scan chains [Chakraborty, Bhawmik, Chiang – TECS'00]
- *NP*-hard, Bin Design heuristics [Marinissen, Goel, Lousberg – ITC'00]
- Minimizing test time and TAM width, Best-Fit Decreasing heur. [Iyengar, Chakrabarty, Marinissen – JETTA'02]

6. Classification of Problems and Prior Work

3. Test Access Mechanism Design

- Multiplexed access [Immaneni & Raman – ITC'90]
- Core transparency [Marinissen et al. – ETC'93] [Ghosh et al. – DAC'98] [Chakrabarty et al. – ICVD'01] [Yoneda & Fujiwara – ATS'01]
- Hierarchical TAM structure [Chakraborty et al. – TECS'00]
- Cores with and without TAPs [Benabdenbi – DATE'01]
- Hierarchical BIST [Benso et al. – ITC'99 / ITC'00]
- Reusing existing system bus [Harrod – ITC'99]
- Dedicated scalable bus-based TAMs
  - Tri-stateable test bus [Varma & Bhatia – ITC'98]
  - Daisychainable TestRail [Marinissen et al. – ITC'98]
  - CAS-BUS [Benabdenbi et al. – DATE'00]

6. Classification of Problems and Prior Work

4. TAM Optimization

- **Basic TAM architectures** [Aerts & Marinissen – ITC'98]
- **Test time minimization through ILP** [Chakrabarty VTS'00]
- **Add routing and power constraints** [Chakrabarty – DAC'00]
- **Replace ILP by genetic algorithm** [Ebadi & Ivanov – ATS'01]

6. Classification of Problems and Prior Work

5. Test Scheduling

- **Combinatorial optimization** [Sugihara et al. – ITC'98]
- **Early-abort reordering** [Jiang & Vinnakota – VTS'99]
- **Test protocol scheduling** [Marinissen & Lousberg – ETW'99]
- **Integer Linear Programming (ILP)** [Chakrabarty – TCAD'00]
- **Power-constrained**
  [Zorian – VTS'93] [Chou et al. – TVLSI'97]
  [Muresan et al. – ITC'00] [Rosinger et al. – ISCAS'01]
  [Larsson & Peng – ATS'01] [Flottes et al. – VLSI'01]
- **Preemptive scheduling with precedence and power constraints**
  [Iyengar & Chakrabarty – VTS'01]

6. Classification of Problems and Prior Work

Combinations

6. TAM Optimization + Test Scheduling
- Combination of TAM optimization and test scheduling [Larsson & Peng – DATE'01] [Nourani & Papachristou – ITC'00]
- Rectangle packing [Huang et al. – ATS'01 / ASP-DAC'02]
- Average time, bipartite graph matching [Koranne – ASP-DAC'02]

7. Integrated TAM & Wrapper Optimization + Test Scheduling
- ILP + exhaustive enumeration [Iyengar et al. – JETTA'02]
- Efficient heuristics [Iyengar et al. – DATE'02]
- Rectangle packing [Iyengar et al. – VTS'02]
- Add precedence, power, preemption constraints [Iyengar et al. – DAC'02]

6. Classification of Problems and Prior Work

'Open' Problems

- Minimization of ATE reloads
- Scheduling of interconnect (ExTest) tests
- Hierarchical TAM optimization, multi-level TAMs
- Test scheduling for hierarchical SOCs
- TAM wire length minimization

7. Conclusion

- Goals *'ITC'02 SOC Test Benchmarks'*
  - Stimulate research into modular SOC testing
  - Make realistic SOC data available to (academic) researchers
  - Enable objective comparison of research results
- Presented
  - Benchmark format
  - Benchmark naming
  - Benchmark set and some characteristics
  - Problems that can be addressed using these benchmarks

Acknowledgements

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- Rubin Parekhji – Texas Instruments
- Erwin Waterlander – Philips Research
- Cheng-Wen Wu – National Tsing Hua University

Parser for .soc Benchmark Format
- Sandeep Kumar Goel – Philips Research

E-mail Reflector
- Bart Vermeulen – Philips Research

And Finally…

- **For Information + Benchmark Download**
  http://www.extra.research.philips.com/itc02socbenchm
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  socbmrks@natlab.research.philips.com
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  erik.jan.marinissen@philips.com