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Panel Summaries

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How useful are the ITC 02 SoC test benchmarks?

THE SIXTH IEEE International Workshop on Testing Embedded Core-Based System Chips (TECS) took place 1-2 May 2002, in Monterey, California. Held in conjunction with the IEEE VLSI Test Symposium, TECS focuses on challenges and emerging solutions related to testing large system chips containing embedded, reusable IP cores.

A panel session organized by Erik Jan Marinissen discussed the usefulness of the ITC 02 test benchmarks for stimulating research in the modular plug-and-play testing of core-based systems on chips (SoCs). Marinissen, along with Duke University's Vikram Iyengar and Krishnendu Chakrabarty, initiated these benchmarks to provide a common set of SoC data for evaluating new methods and tools for SoC testing. These benchmarks have been released to the community via http://www.extra.research.philips.com/itc02socbenchm/, and will be presented at the International Test Conference in October 2002.

Under moderator Krishnendu Chakrabarty, six panelists shared their views. Panelists Chakrabarty, André Ivanov (University of British Columbia), and Sandeep Koranne (Tanner Research) represented benchmark users. Paul Reuter (Mentor Graphics), Brion Keller (IBM), and Steve Pateras (LogicVision) represented potential benchmark providers and potential users of research results. The panel's goal was to reflect the views, needs, and expectations of the community of users, and of the industry experts who are likely to play a key role in making these benchmarks available.

Chakrabarty began the discussion by providing an overview of the benchmarks initiative. He explained that the research community lacks a common set of benchmarks to evaluate and compare algorithms and tools. SoC test automation has received much attention recently, and many research groups published articles on the topic. But in most cases, these groups used only artificial examples rather than real industry SoCs. Moreover, none of the SoC examples were shared by multiple research groups. For example, articles coauthored by researchers at Duke University and Philips Research Labs examined SoCs from Philips; Linköping University in Sweden used an Ericsson SoC in its experiments; and researchers at the University of Iowa and Mentor Graphics used SoCs from Mentor Graphics customers. These different SoCs have thus far prevented an objective evaluation and comparison of the various research claims.

Chakrabarty then presented the ITC 02 SoC benchmark format and naming convention, describing some benchmarks in more detail. He emphasized that these benchmarks are limited to plug-and-play modular testing; they're not intended for fault modeling, fault diagnosis, or testing using merged cores. Finally, Chakrabarty provided a list of test automation

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problems that will benefit from the availability of these benchmarks. These problems include the design and optimization of test access mechanisms (TAMs), test planning and scheduling, and test resource optimization (for example, tester data management).

Ivanov remarked that without SoC test benchmarks, results from SoC testing projects might not be useful to the community. Moreover, only academics will win, because they can continue to write incremental articles and survive in the publish-or-perish culture. In industry, however, it will be impossible to evaluate the effectiveness and efficiency of proposed SoC testing methods without benchmarks. The community will be the real loser because there will be many useless reinventions, lower overall quality, and a lack of reproducibility. With these benchmarks, contended Ivanov, both groups can benefit from new research. In fact, the benchmarks are critical to the major SoC test initiative currently under way at the University of British Columbia.

Sandeep Koranne presented a summary of his SoC testing research (part of which he did while at Philips Research) in which he has used the ITC 02 SoC test benchmarks. He cited several recent SoC testing advances in scheduling and DFT. He said that constructive competition among research groups working on independent ideas but having the same set of test data for validation, communication, and ia exchange have facilitated these advancements. Koranne also presented examples of several successful benchmarking efforts that have spurred research, publications, and technology development. The lack of a set of benchmark circuits is an obstacle to similar progress in SoC testing. The availability of the benchmarks will let more groups and individuals contribute to this field.

Reuter said that the ITC 02 benchmarks do not contain enough information to solve relevant SoC test automation problems. He disputed the claim on the benchmark Web page that you can use these benchmarks to design test wrappers, perform test scheduling, and optimize TAMs. He emphasized that wrapper design requires core interface information, such as signal types, data rates, and information about the relationships between signals. Furthermore, TAM design needs test mode information, such as signals for test modes. The benchmark sizes do not reflect industry state of the art, he said. We need enough data to write IEEE P1450.6 Core Test Language (CTL) for cores, and we need larger SoCs. Obscuring the real core names, internal details of the cores, and pattern information can protect the IP of SoC providers.

Keller tended to agree with Reuter, and explained why he thinks the ITC 02 benchmarks do not contain enough information to be useful. He said it is important to include clock domain information in the benchmark files. It is not possible to schedule test without adequate knowledge of the clocking schemes or the clock domains. Furthermore, if the benchmarks' usefulness is not properly established—for example, by including enough information about the SoC and the embedded cores—motivating designers and DFT engineers to contribute benchmarks will be difficult.

Unlike the other panelists, Pateras contended that there is no need to develop a set of benchmarks using real SoCs from industry. Researchers can simply generate random SoCs using parameters such as the number of I/Os, scan chains, and test patterns. It is not realistic to expect designers to provide all the information needed to make the benchmarks useful.

In the discussion that followed with the audience, the important topics of benchmark content and benchmark format surfaced several times. Several people commented that it is unrealistic to expect companies to release all the information mentioned in the panelists' wish lists. Some audience members remarked that the benchmarks should be available in CTL format because that language is designed to play a standard role in core test information transfer. Panelists and audience participants did, however, agree that the benchmark effort is timely and important. They also agreed that there should be greater interaction at other forums to determine what information the benchmark description should include. ■