ITC'02 SOC Test Benchmarks

Krishnendu Chakrabarty
Department of Electrical & Computer Engineering
Duke University

Co-initiators: Erik Jan Marinissen, Philips Research
Vikram Iyengar, Duke University

Motivation

- Stimulate research into new methods and tools for modular testing of core-based SOCs
- Enable objective comparison of such methods and tools with respect to effectiveness and efficiency
- The research community lacks a common set of benchmarks
- SOCs are made available to research groups on an exclusive basis
  - Duke University (Philips SOCs)
  - Linkoping University, Sweden (Ericsson SOC)
  - University of Iowa (SOCs from customers of Mentor Graphics)

Outline

- Define the benchmark format, naming scheme, and present the benchmark SOCs
- Combine the strengths of both the ISCAS and ITC'99 benchmark sets
  - Strive for a homogeneous set of circuits
  - Include circuits that are representative of today's SOC designs
- Provide an overview of research problems that can be addressed and evaluated by means of this benchmark set
  - Design of optimized test access infrastructures
  - Test scheduling
  - Test resource optimization (e.g. tester data management)

How can I use these benchmarks?

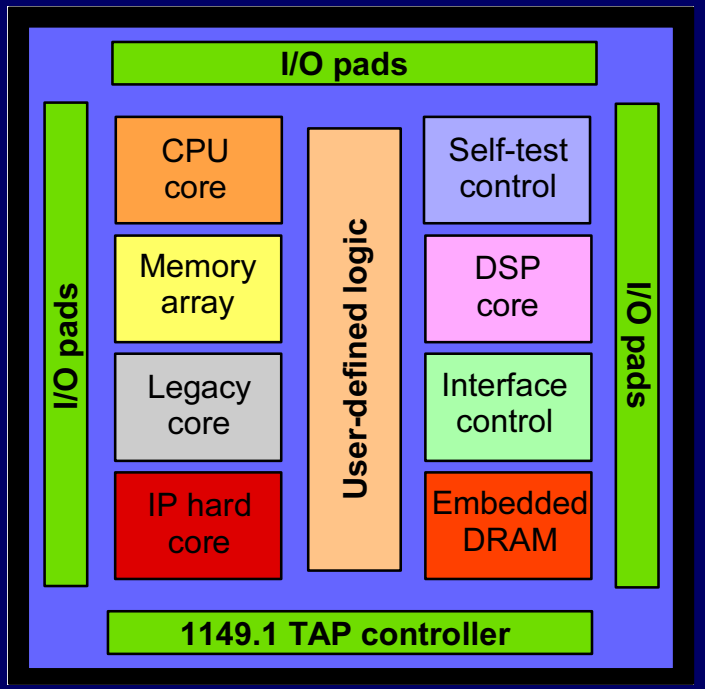
- Use is limited in scope to problems that involve modular plug-and-play testing of SOCs
  - Test planning and SOC-level test development during system integration
- Not intended for evaluating test methods that require detailed internal structure
  - Fault modeling, fault diagnosis, and test generation using merged cores.

Example SOCs

ITC'02 SOC test benchmark initiative

http://www.extra.research.philips.com/itc02socbenchm

- d695 (Duke University)
  - 2 ISCAS'85 benchmark "cores"
  - 8 ISCAS'89 benchmark "cores"
- p22810 (Philips Research)
  - 22 logic cores + 6 memory cores
- p34392 (Philips Research)
  - 4 logic cores + 15 memory cores
- p93791 (Philips Research)
  - 14 logic cores + 18 memory cores
- g1096 (University of Stuttgart, Germany)
- u251 (Universidade Federal do Rio Grande do Sul, Porto Alegre,RS, Brazil)



Benchmark Format

The benchmark format contains the following information per SOC:

- The SOC name
- The total number of modules in the SOC
- Global settings that specify whether or not the optional data for layout position and power dissipation are provided

Benchmark Format (Continued)

- Per module in the SOC:
  - The level in the design hierarchy
  - The number of input, output, and bidirectional terminals
  - The number of scan chains and their lengths
  - The absolute layout location of the core (optional)
  - The total number of tests
  - Per test:
    - Whether or not this test uses the core-internal scan chains and/or the core-external TAM
    - The number of test patterns
    - The power dissipation (optional)

Example [x847.soc]

01 SocName x847

02 TotalModules 7

03 Options Power 1 XY 1

04 Module 0 Level 0 Inputs 312 Outputs 312 Bidirs 0 ScanChains 2 : 54 43

05 Module 0 X -1 Y -1

06 Module 0 TotalTests 2

07 Module 0 Test 1 ScanUse 1 TamUse 1 Patterns 43 Power 128

08 Module 0 Test 2 ScanUse 1 TamUse 1 Patterns 32 Power 537

09 Module 1 Level 1 Inputs 10 Outputs 11 Bidirs 12 ScanChains 4 : 20 21 22 23

10 Module 1 X 678 Y 123

11 Module 1 TotalTests 3

12 Module 1 Test 1 ScanUse 1 TamUse 1 Patterns 567 Power 576

13 Module 1 Test 2 ScanUse 1 TamUse 1 Patterns 876 Power 275

14 Module 1 Test 3 ScanUse 1 TamUse 1 Patterns 908 Power 123

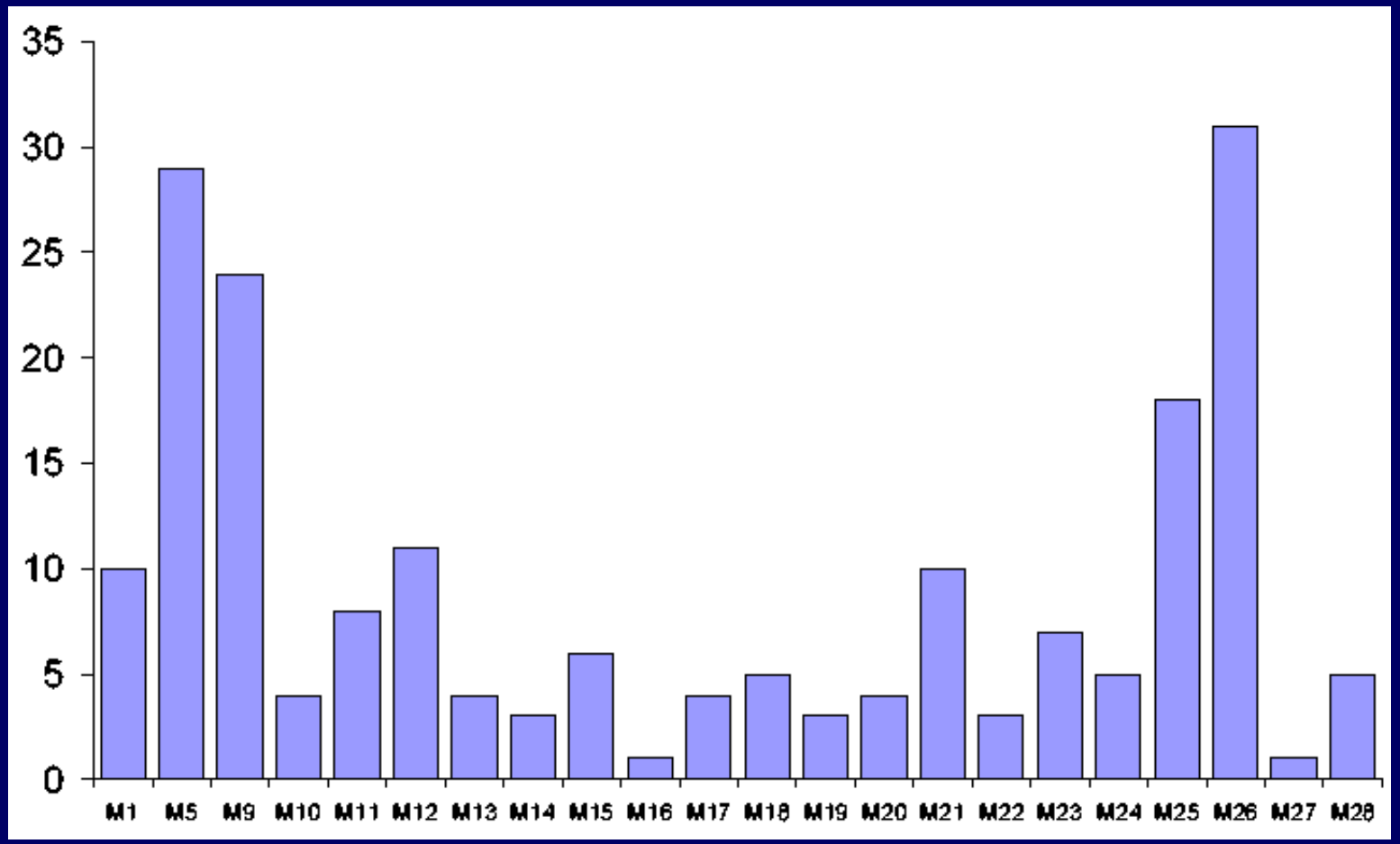
Example [x847.soc] (Contd.)

```
15 Module 2 Level 1 Inputs 44 Outputs 46 Bidirs 0 ScanChains 1 : 100
16 Module 2 X 324 Y 98
17 Module 2 TotalTests 2
18 Module 2 Test 1 ScanUse 1 TamUse 1 Patterns 4356 Power 1334
19 Module 2 Test 2 ScanUse 1 TamUse 1 Patterns 56 Power 2245
20 Module 3 Level 2 Inputs 312 Outputs 312 Bidirs 0 ScanChains 2 : 75
75
21 Module 3 X 304 Y 80
22 Module 3 TotalTests 1
23 Module 3 Test 1 ScanUse 1 TamUse 1 Patterns 25 Power -1
24 Module 4 Level 3 Inputs 112 Outputs 543 Bidirs 23 ScanChains 0 :
25 Module 4 X -1 Y -1
26 Module 4 TotalTests 1
27 Module 4 Test 1 ScanUse 1 TamUse 0 Patterns 12 Power -1
```

Example [x847.soc] (Contd.)

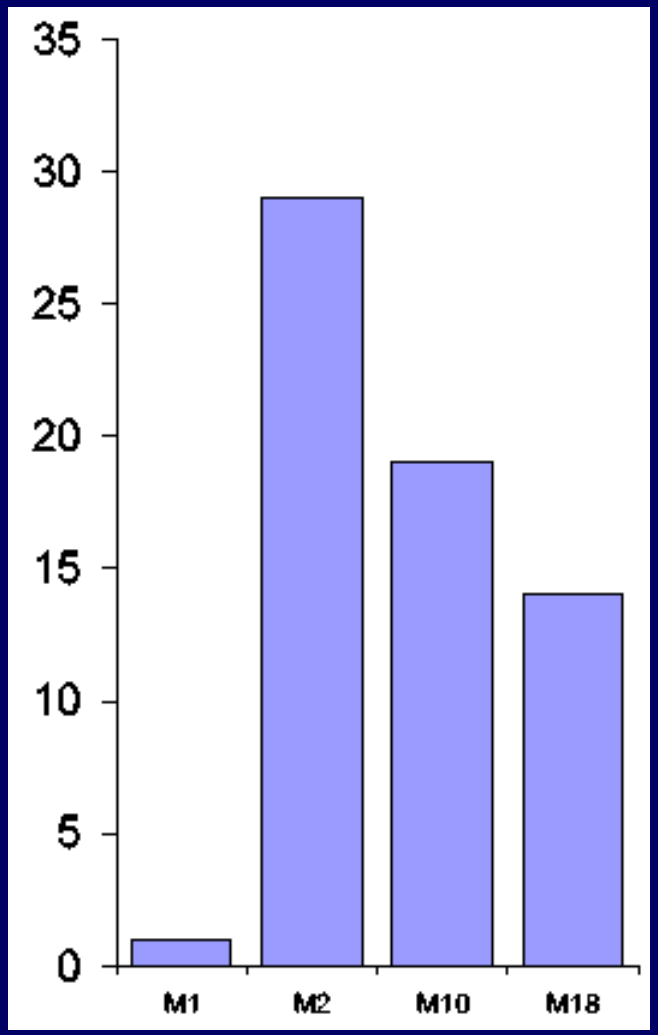
```
28 Module 5 Level 2 Inputs 312 Outputs 312 Bidirs 0 ScanChains 2
: 75 75

29 Module 5 X 344 Y 80

30 Module 5 TotalTests 1

31 Module 5 Test 1 ScanUse 1 TamUse 1 Patterns 25 Power -1

32 Module 6 Level 3 Inputs 112 Outputs 543 Bidirs 23 ScanChains
0 :

33 Module 6 X -1 Y -1

34 Module 6 TotalTests 1

35 Module 6 Test 1 ScanUse 1 TamUse 0 Patterns 12 Power -1
```

Some Details of the Benchmarks



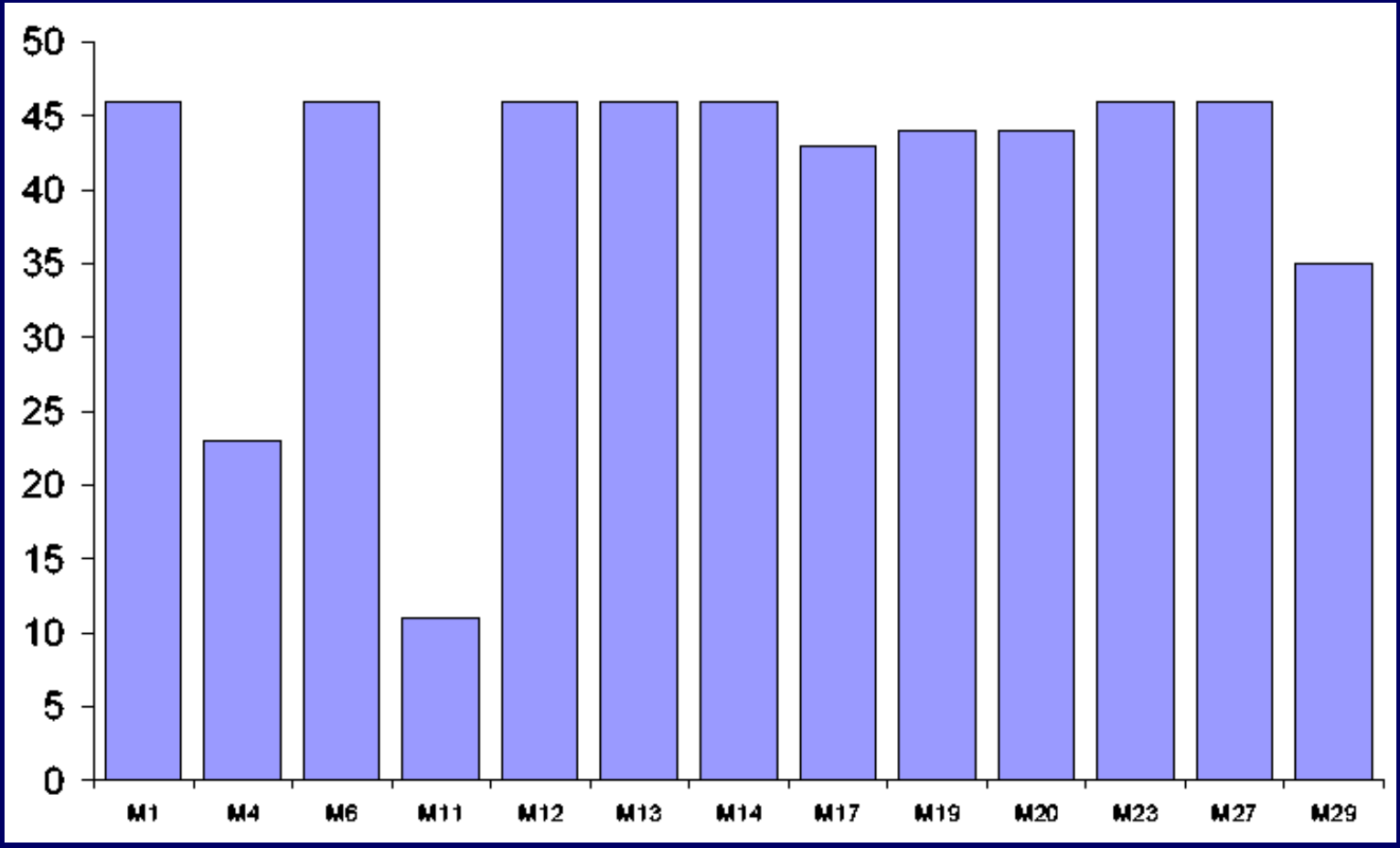
No. of scan chains in the modules in p22810

Some Details of the Benchmarks



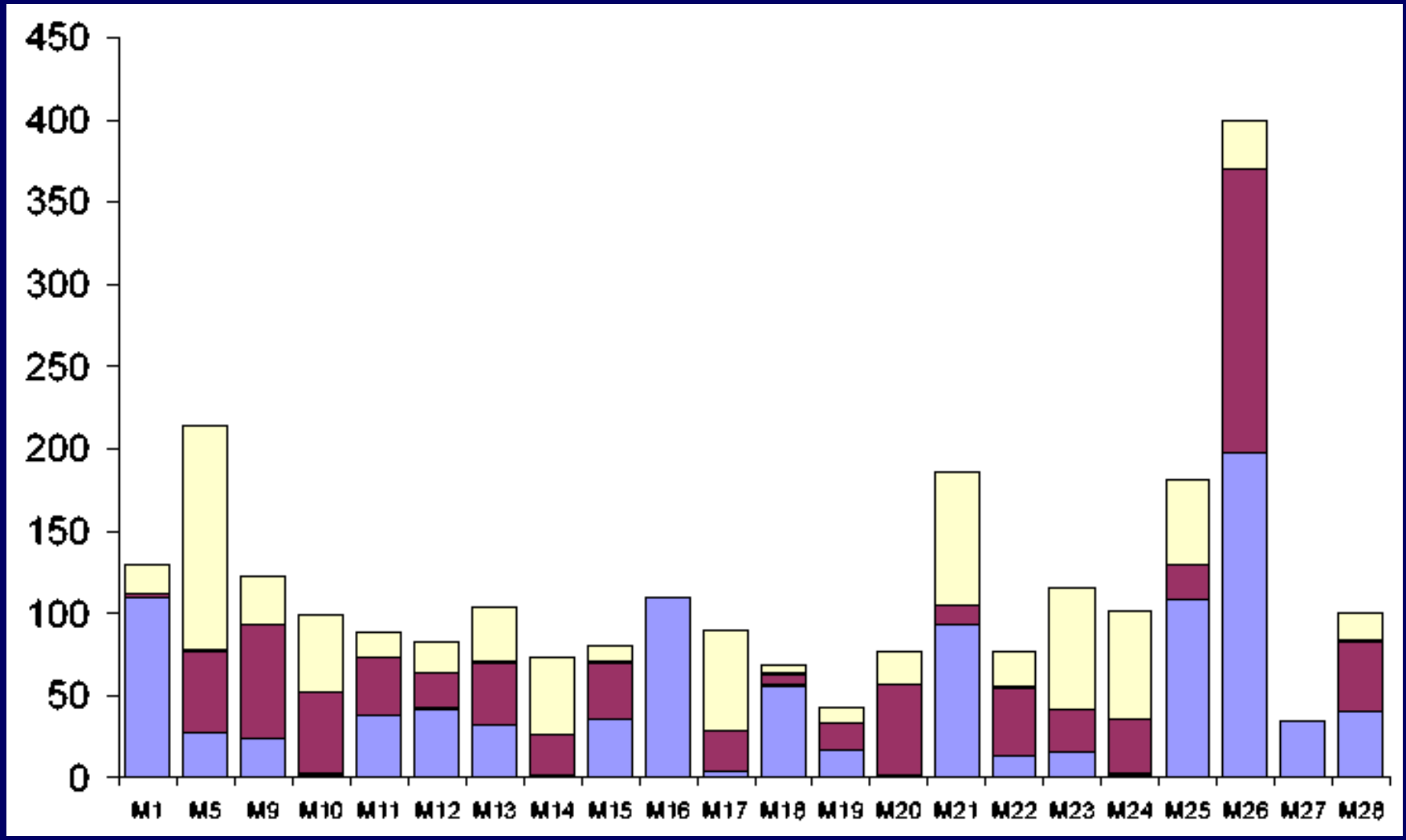
No. of scan chains in the modules in p34392

Some Details of the Benchmarks

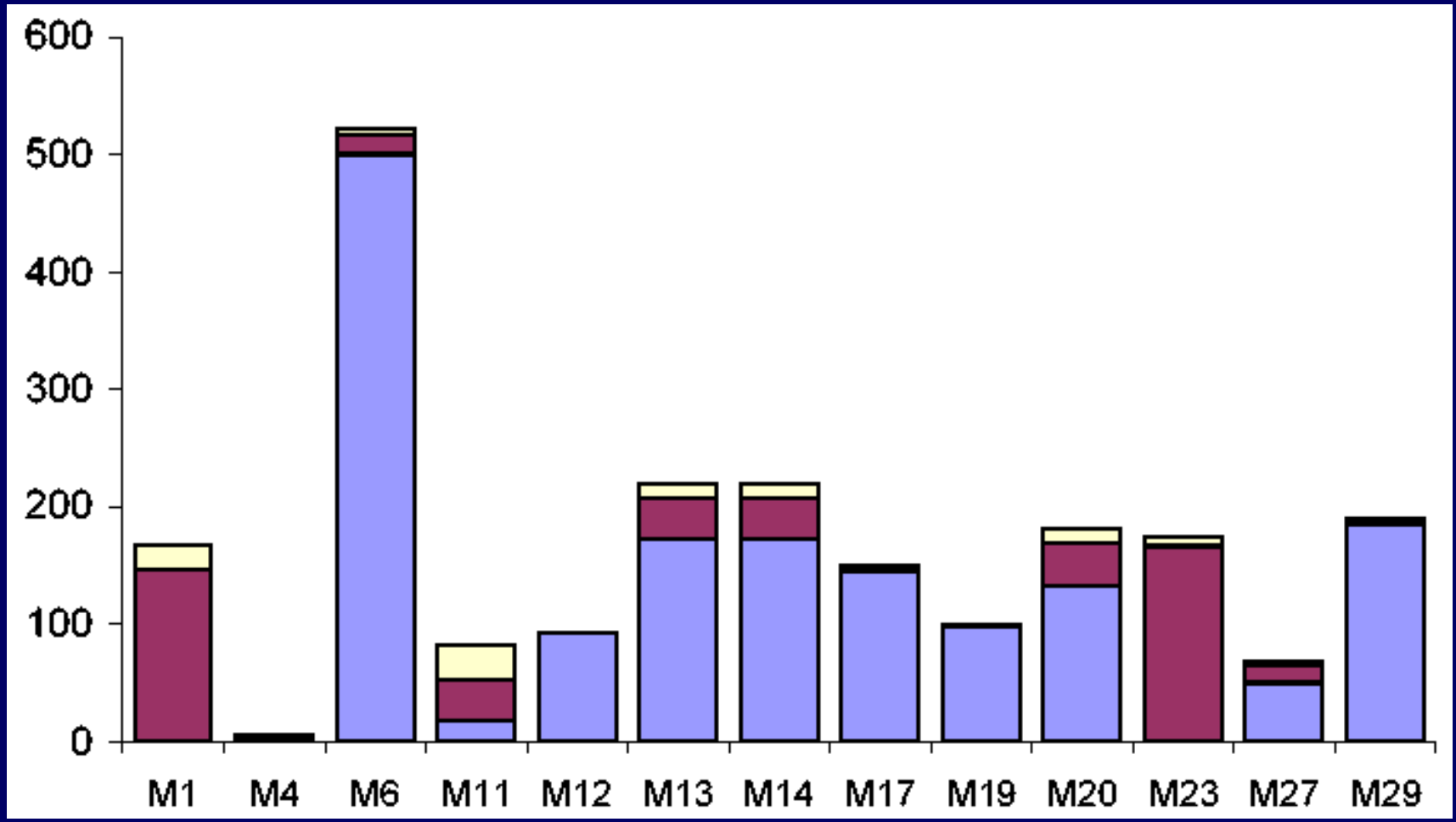


No. of scan chains in the modules in p93791

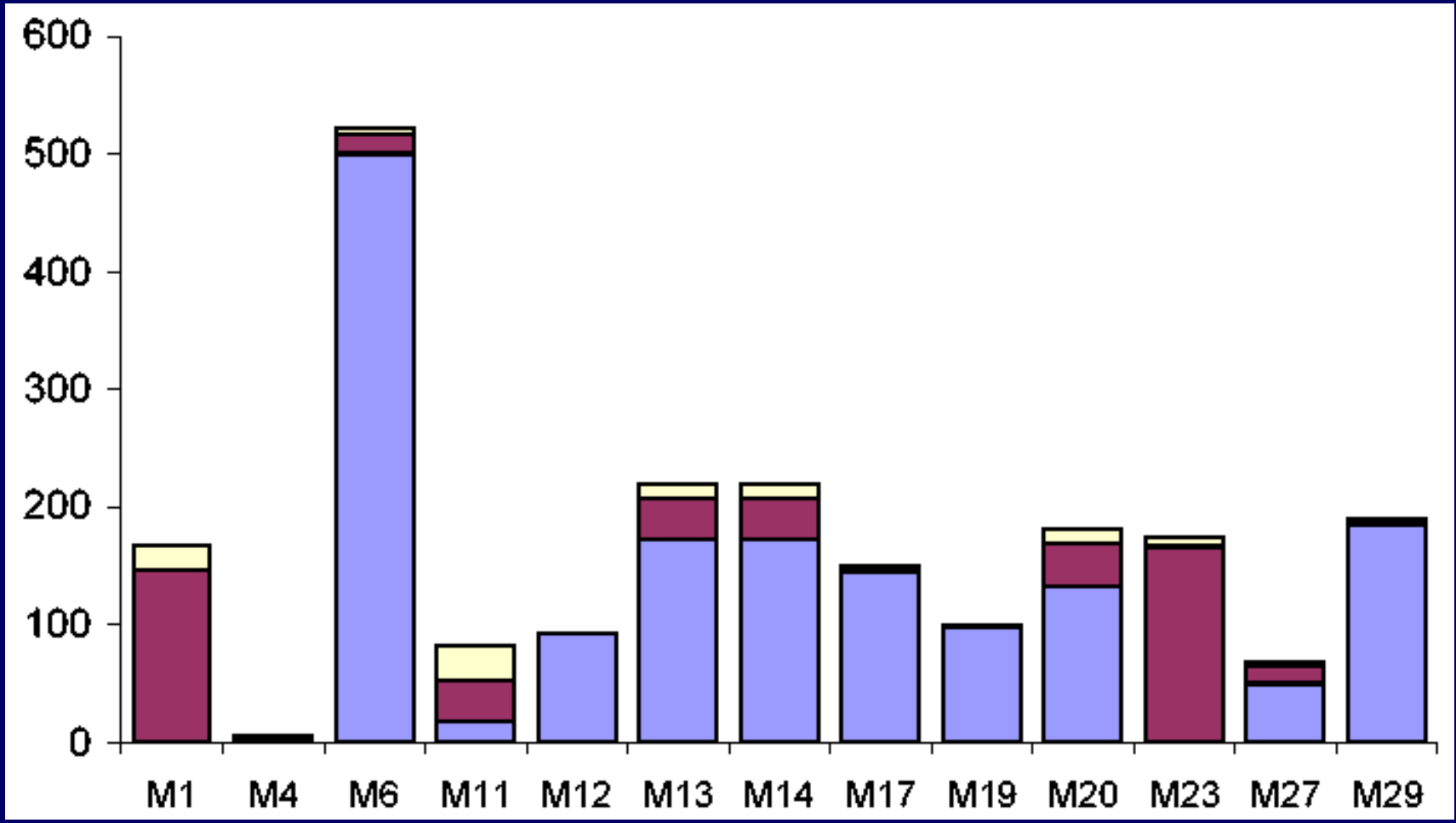
Distribution of Scan Chain Lengths: p22810



Distribution of Scan Chain Lengths: p34392



Distribution of Scan Chain Lengths: p93791



Research Problems in SOC Test Automation

- Test wrapper design & optimization
- TAM design & optimization
- Test scheduling
- Integrated TAM optimization and test scheduling
- Integrated Wrapper/TAM co-optimization and test scheduling
- Test resource optimization
  - Managing tester data volume

Acknowledgements

- Erika Cota, Universidade Federal do Rio Grande do Sul (Porto Alegre, Brazil),
- Rainer Dorsch, University of Stuttgart (Stuttgart, Germany),
- Graeme Francis, Philips Semiconductors (Southampton, United Kingdom)
- Erwin Waterlander, Philips Research (Eindhoven, The Netherlands)